

Compal Confidential

Model Name : AIZY0  
File Name : LA-B921PR10  
BOM P/N:43xxxxxxxx

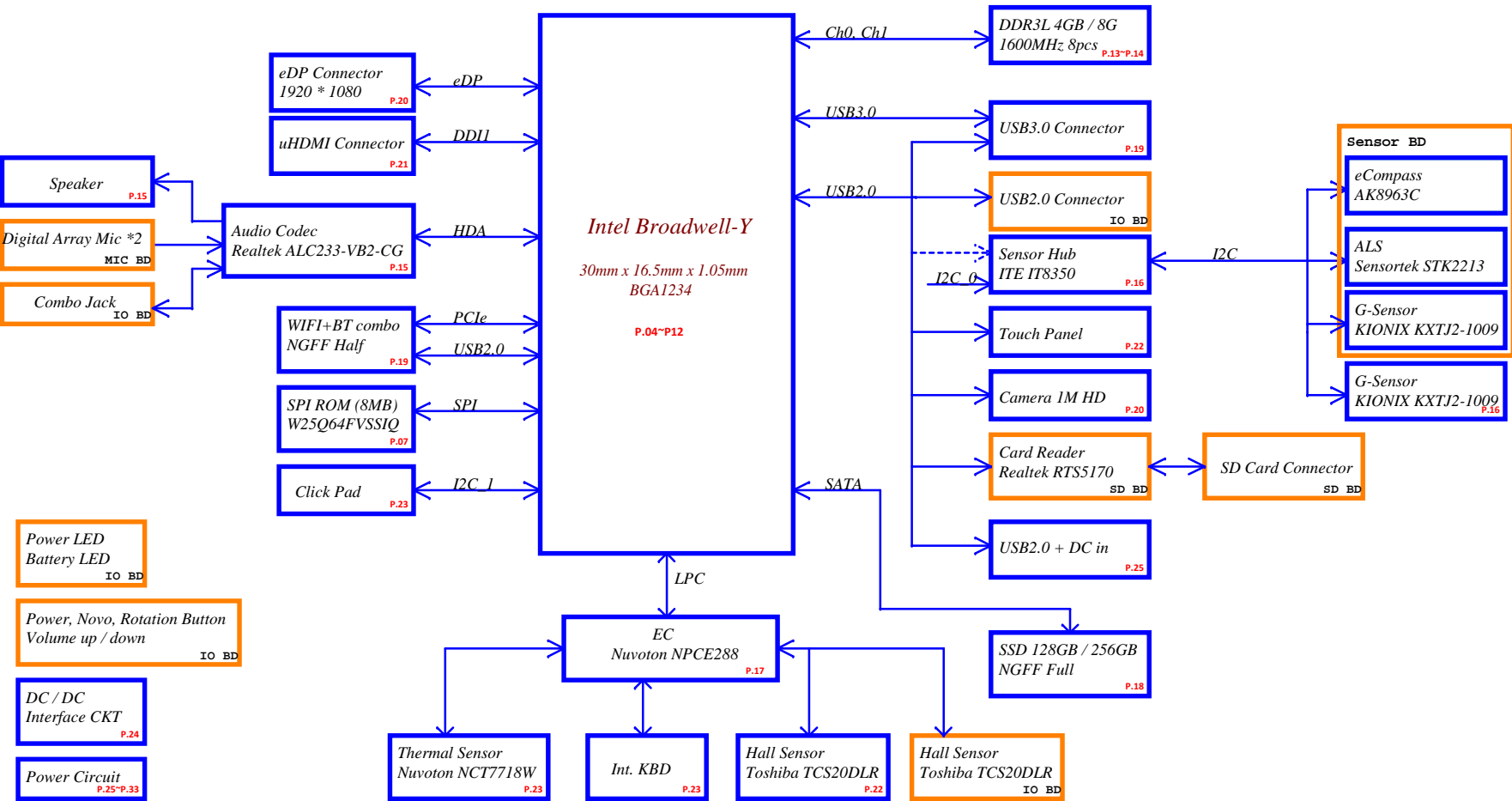
Compal Confidential

AIZY0 M/B Schematics Document  
Intel Broadwell Y Processor

2014-09-30  
REV:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Cover Page	
				Size	Document Number
				Custom	LA-B921PR10
				Date	Rev
				Friday, October 17, 2014	1.0
				Sheet	1 of 36

AIZY0 Intel Broadwell Y Block Diagram



## Voltage Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
UNPOP	@
CPU OPTION	CPU1@ ~ CPU8@
DRAM Option	H4G@ E4G@ S4G@ M4G1@ S8G@ E8G@ H8G@ M8G@ M4G2@
EMI POP	EMI@
ESD POP	ESD@
EMI UNPOP	@EMI@
ESD UNPOP	@ESD@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@

## EC SM Bus1 address

Device	Address
Smart Battery	
Charger	
Home Key Button(TS)	8bit:0x60, 7bit:0x30

## EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001100x
Broadwell ULT SML1	

## CPU SM Bus address

Device	Address
NA	

## CPU SML0 Bus address

Device	Address
NA	

## USB 2.0 Port Table

USB 2.0 Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	DCIN USB COMBO
3	Card Reader
4	Touch Screen
5	Camera
6	Mini Card (WLAN/BT)
7	Sensor Fusion

## USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

## PCIe Port Table

Port	Lane	
1		
2		
3		
4		NGFF WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

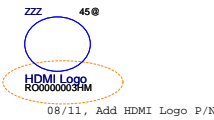
## SATA Port Table

Port	
3	
2	
1	NGFF SSD(SATA)
0	

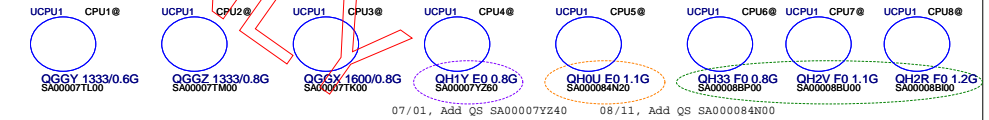
## SMBUS Control Table

	HOST	Changer	BATT	NPCE288	CPU	HomeKey	Thermal sensor NCT7718W
EC_SMB_CK1	NPCE288	+3VLP	+3VLP	X	X	+3VALW	X
EC_SMB_DA1	NPCE288	X	X	X	X	X	X
EC_SMB_CK2	NPCE288	X	X	X	X	X	X
EC_SMB_DA2	NPCE288	X	X	X	X	X	X
SMBCLK	CPU	+3VALW	X	X	X	X	X
SMBDATA	CPU	+3VALW	X	X	X	X	X
SML0CLK	CPU	+3VALW	X	X	X	X	X
SML0DATA	CPU	+3VALW	X	X	X	X	X
SML1CLK	CPU	+3VS	X	X	X	X	X
SML1DATA	CPU	+3VS	X	X	X	X	X

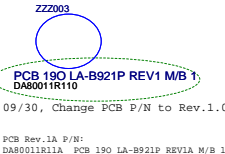
## HDMI Logo



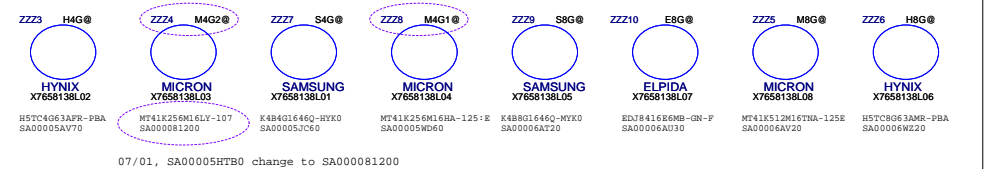
## CPU part



## PCB part



## DRAM

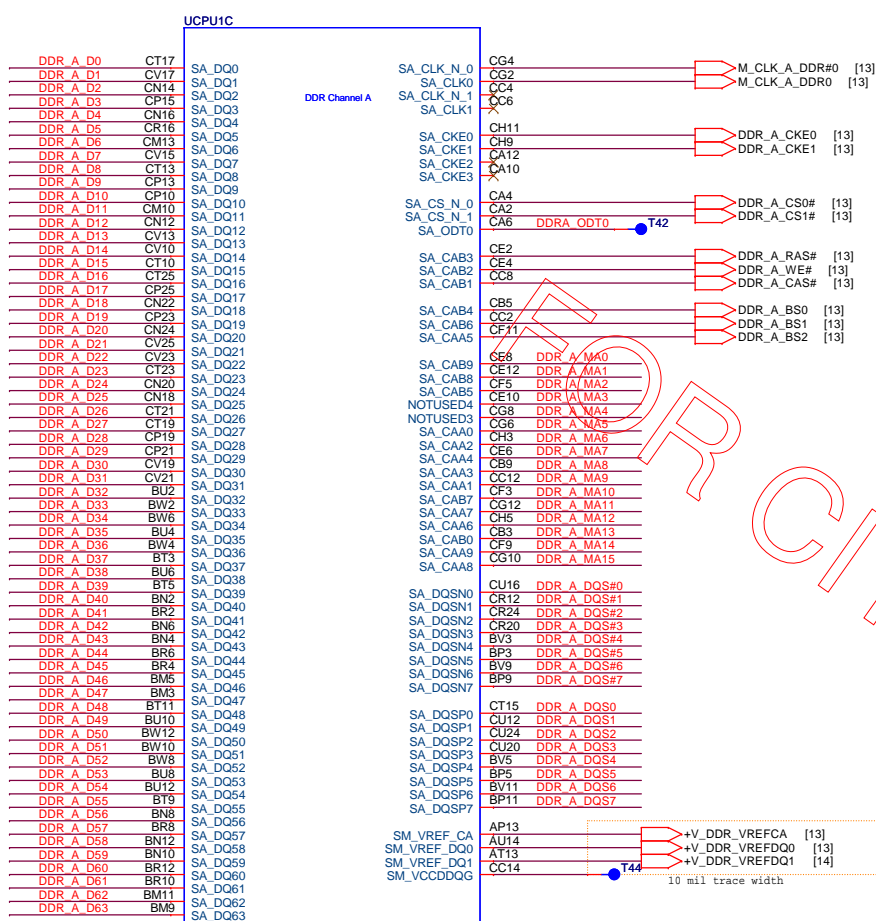


Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2014/04/10	Deciphered Date
2017/04/10		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		
Title		Note List
Size		Document Number
Date		Friday, October 17, 2014
Sheet		3 of 36

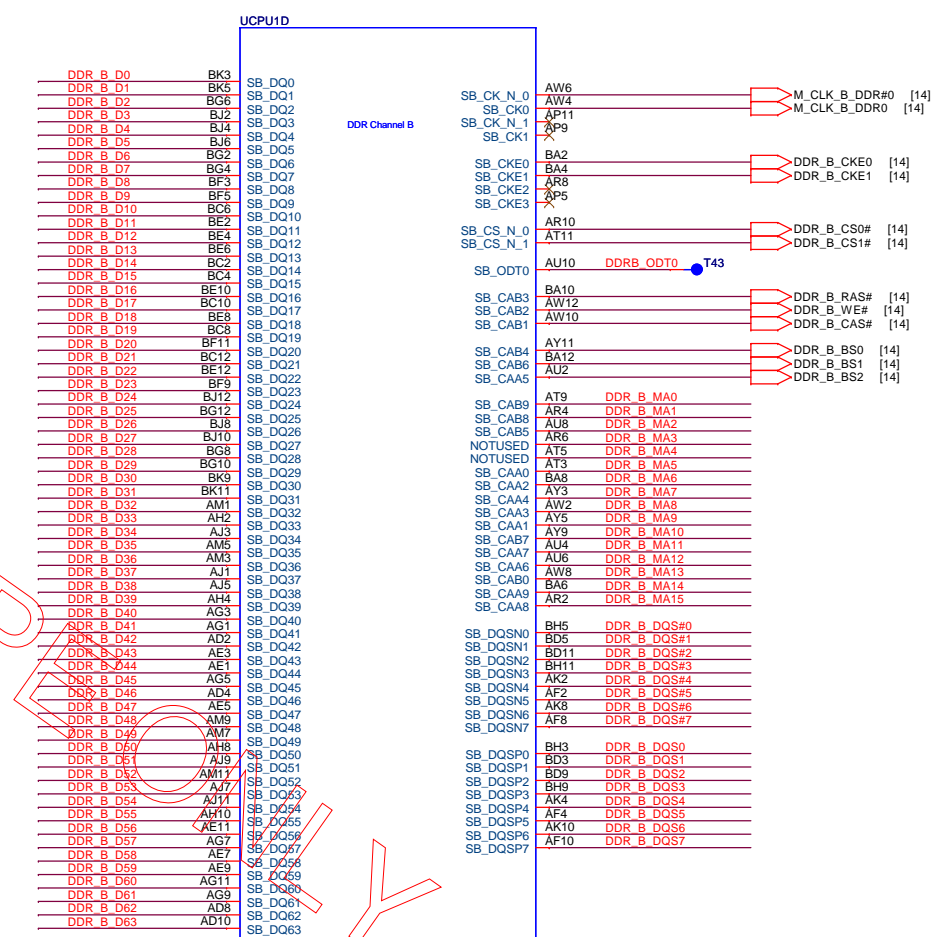


[13] DDR\_A\_D[0..63]  
[13] DDR\_A\_MA[0..15]  
[13] DDR\_A\_DQS#[0..7]  
[13] DDR\_A\_DQS[0..7]

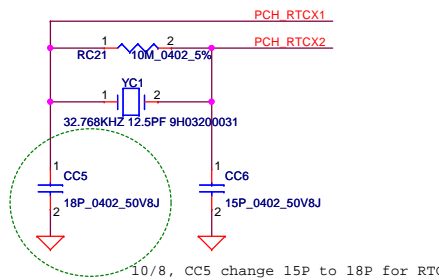
[14] DDR\_B\_D[0..63]  
[14] DDR\_B\_MA[0..15]  
[14] DDR\_B\_DQS#[0..7]  
[14] DDR\_B\_DQS[0..7]



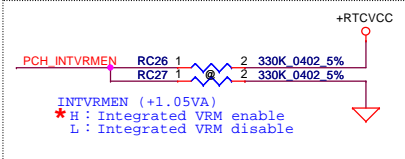
BDW-YLPDDR3\_BGA1234 3 OF 20



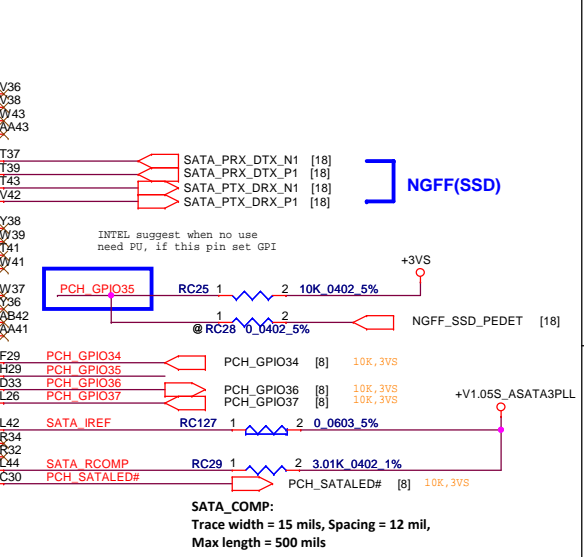
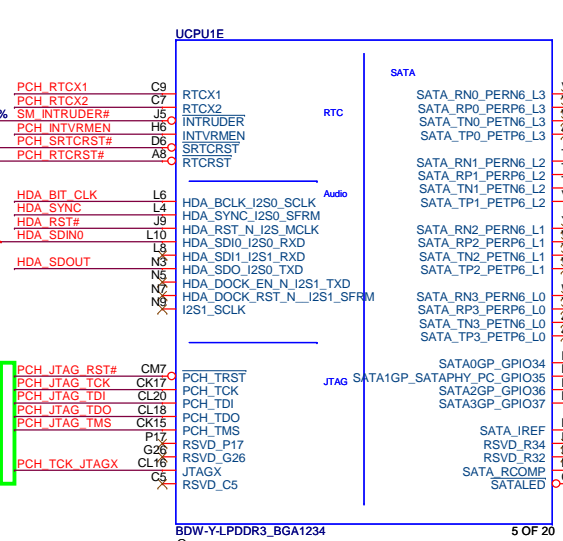
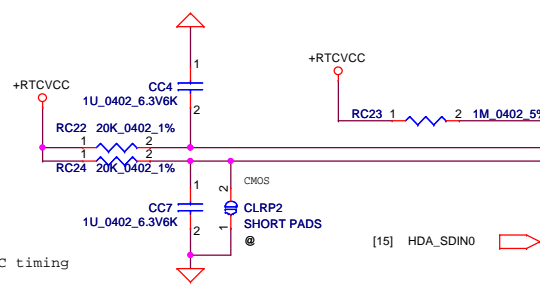
BDW-YLPDDR3\_BGA1234 4 OF 20



10/8, CC5 change 15P to 18P for RTC timing



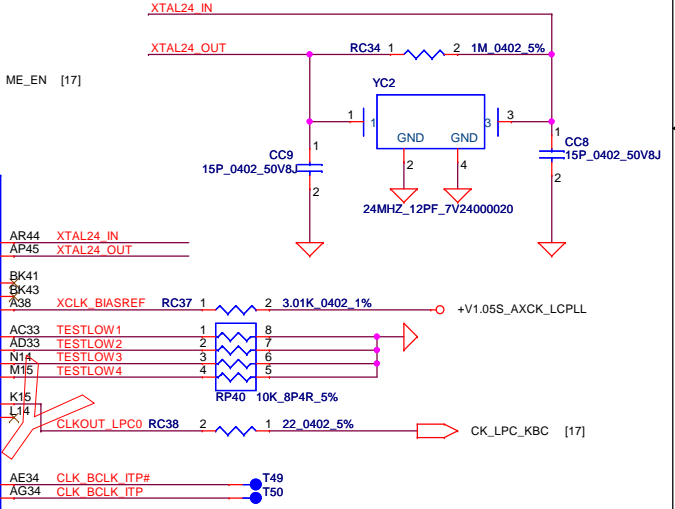
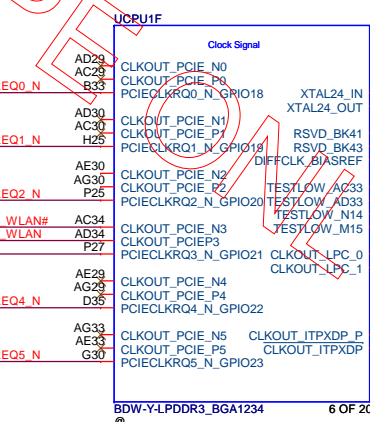
To enable the integrated voltage regulator for DCPUSU1, DCPUSU2, DCPUSU3 and DCPUSU4 this signal must be pulled to VCCRTC through a weak resistor (for example, 330 KΩ ±5%). To disable the integrated voltage regulator, this signal must be pulled down through a weak resistor (for example, 330 KΩ ±5%) and the DCPUS rails must be powered externally.



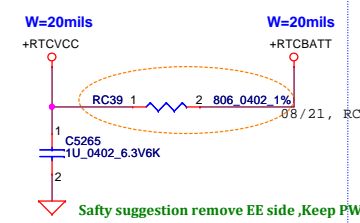
FORCIP

### EMI

- [15] HDA\_RST\_AUDIO#
- [15] HDA\_BITCLK\_AUDIO
- [15] HDA\_SDOOUT\_AUDIO
- [15] HDA\_SYNC\_AUDIO



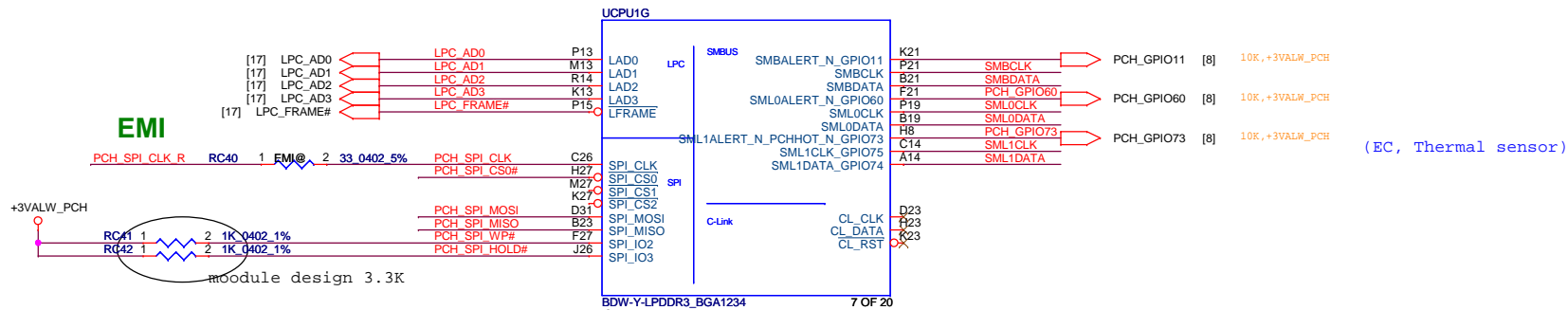
### RTC Battery



08/21, RC39 change to 806 ohm

Safety suggestion remove EE side, Keep PWR side

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	BDW MCP(3/9) SATA,HDA,CLK
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-B921PR10
				Date	Thursday, October 23, 2014
				Rev	1.0
				Sheet	6 of 36

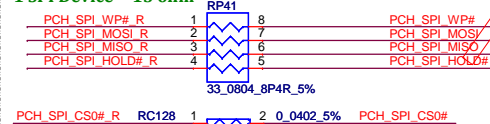


Closed to ROM

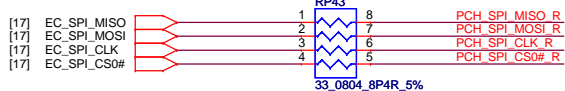
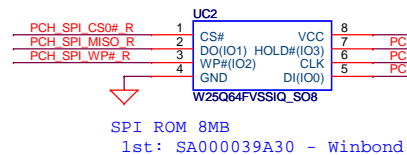
CHKLIST1.0

2 SPI Device = 33 ohm

1 SPI Device = 15 ohm



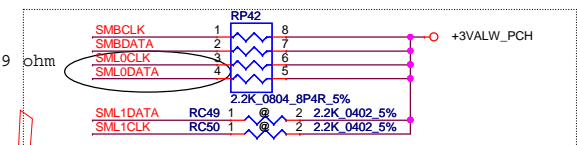
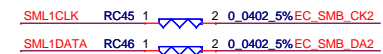
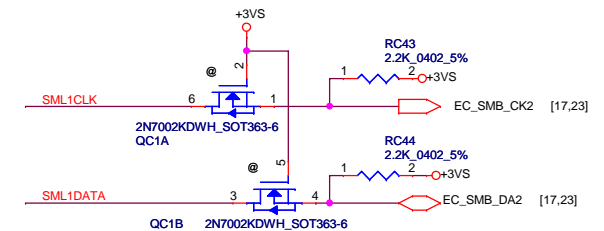
SPI ROM FOR ME ( 8MByte )  
ROM is Quad SPI



SML1 Bus BIOS set Native,  
it's OD pin

SML1 Bus :EC/Thermal Sensor


FootPrint :DMN6D0LDW-7\_SOT363-6



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/04/10				Deciphered Date			
2017/04/10				Title				BDW MCP(4/9) LPC,SPI,SMBUS			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RECD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number				Rev			
LA-B921PR10				1.0				Date:			
Friday, October 17, 2014				Sheet				7 of 36			



**ESD**



The diagram shows an ESD protection circuit. A red dashed rectangle encloses the components. Inside, a blue capacitor is connected between a signal line labeled 'H\_PLT\_RST#' and ground. The capacitor is labeled 'ESD@', 'CC83', and '100P\_0402\_50V8J'. A red triangle symbol is connected to the ground line.

07/07, change to mount



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P08-BDW MCP(5/9) PM,GPIO,I2C</b>		
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Customer	<b>LA-B921PR10</b>	1.0
				Date:	Friday, October 17, 2014	Sheet 8 of 36



WLAN

[19] PCIE\_PRX\_DTX\_N4  
[19] PCIE\_PRX\_DTX\_P4  
[19] PCIE\_PTX\_C\_DRX\_N4  
[19] PCIE\_PTX\_C\_DRX\_P4

+V1.05S\_AUSB3PLL

PCIE\_RCOMP:  
Trace width = 15 mils, Spacing = 15 mil,  
Max length = 500 mils

TP\_F3\_H2  
TP\_F45\_F43  
TP\_F3\_H2  
TP\_H44

T63

UCPU1K

AF40 PERN5\_L0  
AG41 PERP5\_L0  
AU40 PETN5\_L0  
AU42 PETP5\_L0  
AD40 PERN5\_L1  
AE41 PERP5\_L1  
AW40 PETN5\_L1  
AW42 PETP5\_L1  
AE43 PERN5\_L2  
AD42 PERP5\_L2  
BA42 PETN5\_L2  
BA40 PETP5\_L2  
AF42 PERN5\_L3  
AG43 PERP5\_L3  
BB41 PETN5\_L3  
BB43 PETP5\_L3  
AD38 PERN3  
AC39 PERP3  
AY41 PETN3  
AY43 PETP3  
AH38 PERN4  
AH40 PERP4  
AV41 PETN4  
AV43 PETP4  
AF38 PERN1\_USB3RN3  
AE39 PERP1\_USB3RP3  
BD41 PETN1\_USB3TN3  
BD43 PETP1\_USB3TP3  
AH42 PERN2\_USB3RN4  
AJ43 PERP2\_USB3RP4  
BC40 PETN2\_USB3TN4  
BC42 PETP2\_USB3TP4  
AT41 RSVD\_AT41  
AT43 RSVD\_AT43  
C41 PCIE\_RCOMP  
C41 PCIE\_REF

PCIE\_PRX\_DTX\_N4  
PCIE\_PRX\_DTX\_P4  
PCIE\_PTX\_DRX\_N4  
PCIE\_PTX\_DRX\_P4

CC17 1 2 0.1U 0402 16VK7  
CC18 1 2 0.1U 0402 16VK7

PCIE\_PTX\_DRX\_N4  
PCIE\_PTX\_DRX\_P4

PERN1\_USB3RN3  
PERP1\_USB3RP3  
PETN1\_USB3TN3  
PETP1\_USB3TP3

PERN2\_USB3RN4  
PERP2\_USB3RP4  
PETN2\_USB3TN4  
PETP2\_USB3TP4

RSVD\_AT41  
RSVD\_AT43  
PCIE\_RCOMP  
PCIE\_REF

OC0\_N\_GPIO40  
OC1\_N\_GPIO41  
OC2\_N\_GPIO42  
OC3\_N\_GPIO43

RSVD\_V4  
RSVD\_T3  
RSVD\_Y4  
RSVD\_W3

USB3RN1  
USB3RP1  
USB3TN1  
USB3TP1

USB3RN2  
USB3RP2  
USB3TN2  
USB3TP2

USB3RN3  
USB3RP3  
USB3TN3  
USB3TP3

USB3RN4  
USB3RP4  
USB3TN4  
USB3TP4

USB3RN5  
USB3RP5  
USB3TN5  
USB3TP5

USB3RN6  
USB3RP6  
USB3TN6  
USB3TP6

USB3RN7  
USB3RP7  
USB3TN7  
USB3TP7

USB3RN8  
USB3RP8  
USB3TN8  
USB3TP8

USB3RN9  
USB3RP9  
USB3TN9  
USB3TP9

USB3RN10  
USB3RP10  
USB3TN10  
USB3TP10

USB3RN11  
USB3RP11  
USB3TN11  
USB3TP11

USB3RN12  
USB3RP12  
USB3TN12  
USB3TP12

USB3RN13  
USB3RP13  
USB3TN13  
USB3TP13

USB3RN14  
USB3RP14  
USB3TN14  
USB3TP14

USB3RN15  
USB3RP15  
USB3TN15  
USB3TP15

USB3RN16  
USB3RP16  
USB3TN16  
USB3TP16

USB3RN17  
USB3RP17  
USB3TN17  
USB3TP17

USB3RN18  
USB3RP18  
USB3TN18  
USB3TP18

USB3RN19  
USB3RP19  
USB3TN19  
USB3TP19

USB3RN20  
USB3RP20  
USB3TN20  
USB3TP20

USB3RN21  
USB3RP21  
USB3TN21  
USB3TP21

USB3RN22  
USB3RP22  
USB3TN22  
USB3TP22

USB3RN23  
USB3RP23  
USB3TN23  
USB3TP23

USB3RN24  
USB3RP24  
USB3TN24  
USB3TP24

USB3RN25  
USB3RP25  
USB3TN25  
USB3TP25

USB3RN26  
USB3RP26  
USB3TN26  
USB3TP26

USB3RN27  
USB3RP27  
USB3TN27  
USB3TP27

USB3RN28  
USB3RP28  
USB3TN28  
USB3TP28

USB3RN29  
USB3RP29  
USB3TN29  
USB3TP29

USB3RN30  
USB3RP30  
USB3TN30  
USB3TP30

USB3RN31  
USB3RP31  
USB3TN31  
USB3TP31

USB3RN32  
USB3RP32  
USB3TN32  
USB3TP32

USB3RN33  
USB3RP33  
USB3TN33  
USB3TP33

USB3RN34  
USB3RP34  
USB3TN34  
USB3TP34

USB3RN35  
USB3RP35  
USB3TN35  
USB3TP35

USB3RN36  
USB3RP36  
USB3TN36  
USB3TP36

USB3RN37  
USB3RP37  
USB3TN37  
USB3TP37

USB3RN38  
USB3RP38  
USB3TN38  
USB3TP38

USB3RN39  
USB3RP39  
USB3TN39  
USB3TP39

USB3RN40  
USB3RP40  
USB3TN40  
USB3TP40

USB3RN41  
USB3RP41  
USB3TN41  
USB3TP41

USB3RN42  
USB3RP42  
USB3TN42  
USB3TP42

USB3RN43  
USB3RP43  
USB3TN43  
USB3TP43

USB3RN44  
USB3RP44  
USB3TN44  
USB3TP44

USB3RN45  
USB3RP45  
USB3TN45  
USB3TP45

USB3RN46  
USB3RP46  
USB3TN46  
USB3TP46

USB3RN47  
USB3RP47  
USB3TN47  
USB3TP47

USB3RN48  
USB3RP48  
USB3TN48  
USB3TP48

USB3RN49  
USB3RP49  
USB3TN49  
USB3TP49

USB3RN50  
USB3RP50  
USB3TN50  
USB3TP50

USB3RN51  
USB3RP51  
USB3TN51  
USB3TP51

USB3RN52  
USB3RP52  
USB3TN52  
USB3TP52

USB3RN53  
USB3RP53  
USB3TN53  
USB3TP53

USB3RN54  
USB3RP54  
USB3TN54  
USB3TP54

USB3RN55  
USB3RP55  
USB3TN55  
USB3TP55

USB3RN56  
USB3RP56  
USB3TN56  
USB3TP56

USB3RN57  
USB3RP57  
USB3TN57  
USB3TP57

USB3RN58  
USB3RP58  
USB3TN58  
USB3TP58

USB3RN59  
USB3RP59  
USB3TN59  
USB3TP59

USB3RN60  
USB3RP60  
USB3TN60  
USB3TP60

USB3RN61  
USB3RP61  
USB3TN61  
USB3TP61

USB3RN62  
USB3RP62  
USB3TN62  
USB3TP62

USB3RN63  
USB3RP63  
USB3TN63  
USB3TP63

USB3RN64  
USB3RP64  
USB3TN64  
USB3TP64

USB3RN65  
USB3RP65  
USB3TN65  
USB3TP65

USB3RN66  
USB3RP66  
USB3TN66  
USB3TP66

USB3RN67  
USB3RP67  
USB3TN67  
USB3TP67

USB3RN68  
USB3RP68  
USB3TN68  
USB3TP68

USB3RN69  
USB3RP69  
USB3TN69  
USB3TP69

USB3RN70  
USB3RP70  
USB3TN70  
USB3TP70

USB3RN71  
USB3RP71  
USB3TN71  
USB3TP71

USB3RN72  
USB3RP72  
USB3TN72  
USB3TP72

USB3RN73  
USB3RP73  
USB3TN73  
USB3TP73

USB3RN74  
USB3RP74  
USB3TN74  
USB3TP74

USB3RN75  
USB3RP75  
USB3TN75  
USB3TP75

USB3RN76  
USB3RP76  
USB3TN76  
USB3TP76

USB3RN77  
USB3RP77  
USB3TN77  
USB3TP77

USB3RN78  
USB3RP78  
USB3TN78  
USB3TP78

USB3RN79  
USB3RP79  
USB3TN79  
USB3TP79

USB3RN80  
USB3RP80  
USB3TN80  
USB3TP80

USB3RN81  
USB3RP81  
USB3TN81  
USB3TP81

USB3RN82  
USB3RP82  
USB3TN82  
USB3TP82

USB3RN83  
USB3RP83  
USB3TN83  
USB3TP83

USB3RN84  
USB3RP84  
USB3TN84  
USB3TP84

USB3RN85  
USB3RP85  
USB3TN85  
USB3TP85

USB3RN86  
USB3RP86  
USB3TN86  
USB3TP86

USB3RN87  
USB3RP87  
USB3TN87  
USB3TP87

USB3RN88  
USB3RP88  
USB3TN88  
USB3TP88

USB3RN89  
USB3RP89  
USB3TN89  
USB3TP89

USB3RN90  
USB3RP90  
USB3TN90  
USB3TP90

USB3RN91  
USB3RP91  
USB3TN91  
USB3TP91

USB3RN92  
USB3RP92  
USB3TN92  
USB3TP92

USB3RN93  
USB3RP93  
USB3TN93  
USB3TP93

USB3RN94  
USB3RP94  
USB3TN94  
USB3TP94

USB3RN95  
USB3RP95  
USB3TN95  
USB3TP95

USB3RN96  
USB3RP96  
USB3TN96  
USB3TP96

USB3RN97  
USB3RP97  
USB3TN97  
USB3TP97

USB3RN98  
USB3RP98  
USB3TN98  
USB3TP98

USB3RN99  
USB3RP99  
USB3TN99  
USB3TP99

USB3RN100  
USB3RP100  
USB3TN100  
USB3TP100

USB3RN101  
USB3RP101  
USB3TN101  
USB3TP101

USB3RN102  
USB3RP102  
USB3TN102  
USB3TP102

USB3RN103  
USB3RP103  
USB3TN103  
USB3TP103

USB3RN104  
USB3RP104  
USB3TN104  
USB3TP104

USB3RN105  
USB3RP105  
USB3TN105  
USB3TP105

USB3RN106  
USB3RP106  
USB3TN106  
USB3TP106

USB3RN107  
USB3RP107  
USB3TN107  
USB3TP107

USB3RN108  
USB3RP108  
USB3TN108  
USB3TP108

USB3RN109  
USB3RP109  
USB3TN109  
USB3TP109

USB3RN110  
USB3RP110  
USB3TN110  
USB3TP110

USB3RN111  
USB3RP111  
USB3TN111  
USB3TP111

USB3RN112  
USB3RP112  
USB3TN112  
USB3TP112

USB3RN113  
USB3RP113  
USB3TN113  
USB3TP113

USB3RN114  
USB3RP114  
USB3TN114  
USB3TP114

USB3RN115  
USB3RP115  
USB3TN115  
USB3TP115

USB3RN116  
USB3RP116  
USB3TN116  
USB3TP116

USB3RN117  
USB3RP117  
USB3TN117  
USB3TP117

USB3RN118  
USB3RP118  
USB3TN118  
USB3TP118

USB3RN119  
USB3RP119  
USB3TN119  
USB3TP119

USB3RN120  
USB3RP120  
USB3TN120  
USB3TP120

USB3RN121  
USB3RP121  
USB3TN121  
USB3TP121

USB3RN122  
USB3RP122  
USB3TN122  
USB3TP122

USB3RN123  
USB3RP123  
USB3TN123  
USB3TP123

USB3RN124  
USB3RP124  
USB3TN124  
USB3TP124

USB3RN125  
USB3RP125  
USB3TN125  
USB3TP125

USB3RN126  
USB3RP126  
USB3TN126  
USB3TP126

USB3RN127  
USB3RP127  
USB3TN127  
USB3TP127

USB3RN128  
USB3RP128  
USB3TN128  
USB3TP128

USB3RN129  
USB3RP129  
USB3TN129  
USB3TP129

USB3RN130  
USB3RP130  
USB3TN130  
USB3TP130

USB3RN131  
USB3RP131  
USB3TN131  
USB3TP131

USB3RN132  
USB3RP132  
USB3TN132  
USB3TP132

USB3RN133  
USB3RP133  
USB3TN133  
USB3TP133

USB3RN134  
USB3RP134  
USB3TN134  
USB3TP134

USB3RN135  
USB3RP135  
USB3TN135  
USB3TP135

USB3RN136  
USB3RP136  
USB3TN136  
USB3TP136

USB3RN137  
USB3RP137  
USB3TN137  
USB3TP137

USB3RN138  
USB3RP138  
USB3TN138  
USB3TP138

USB3RN139  
USB3RP139  
USB3TN139  
USB3TP139

USB3RN140  
USB3RP140  
USB3TN140  
USB3TP140

USB3RN141  
USB3RP141  
USB3TN141  
USB3TP141

USB3RN142  
USB3RP142  
USB3TN142  
USB3TP142

USB3RN143  
USB3RP143  
USB3TN143  
USB3TP143

USB3RN144  
USB3RP144  
USB3TN144  
USB3TP144

USB3RN145  
USB3RP145  
USB3TN145  
USB3TP145

USB3RN146  
USB3RP146  
USB3TN146  
USB3TP146

USB3RN147  
USB3RP147  
USB3TN147  
USB3TP147

USB3RN148  
USB3RP148  
USB3TN148  
USB3TP148

USB3RN149  
USB3RP149  
USB3TN149  
USB3TP149

USB3RN150  
USB3RP150  
USB3TN150  
USB3TP150

USB3RN151  
USB3RP151  
USB3TN151  
USB3TP151

USB3RN152  
USB3RP152  
USB3TN152  
USB3TP152

USB3RN153  
USB3RP153  
USB3TN153  
USB3TP153

USB3RN154  
USB3RP154  
USB3TN154  
USB3TP154

USB3RN155  
USB3RP155  
USB3TN155  
USB3TP155

USB3RN156  
USB3RP156  
USB3TN156  
USB3TP156

USB3RN157  
USB3RP157  
USB3TN157  
USB3TP157

USB3RN158  
USB3RP158  
USB3TN158  
USB3TP158

USB3RN159  
USB3RP159  
USB3TN159  
USB3TP159

USB3RN160  
USB3RP160  
USB3TN160  
USB3TP160

USB3RN161  
USB3RP161  
USB3TN161  
USB3TP161

USB3RN162  
USB3RP162  
USB3TN162  
USB3TP162

USB3RN163  
USB3RP163  
USB3TN163  
USB3TP163

USB3RN164  
USB3RP164  
USB3TN164  
USB3TP164

USB3RN165  
USB3RP165  
USB3TN165  
USB3TP165

USB3RN166  
USB3RP166  
USB3TN166  
USB3TP166

USB3RN167  
USB3RP167  
USB3TN167  
USB3TP167

USB3RN168  
USB3RP168  
USB3TN168  
USB3TP168

USB3RN169  
USB3RP169  
USB3TN169  
USB3TP169

USB3RN170  
USB3RP170  
USB3TN170  
USB3TP170

USB3RN171  
USB3RP171  
USB3TN171  
USB3TP171

USB3RN172  
USB3RP172  
USB3TN172  
USB3TP172

USB3RN173  
USB3RP173  
USB3TN173  
USB3TP173

USB3RN174  
USB3RP174  
USB3TN174  
USB3TP174

USB3RN175  
USB3RP175  
USB3TN175  
USB3TP175

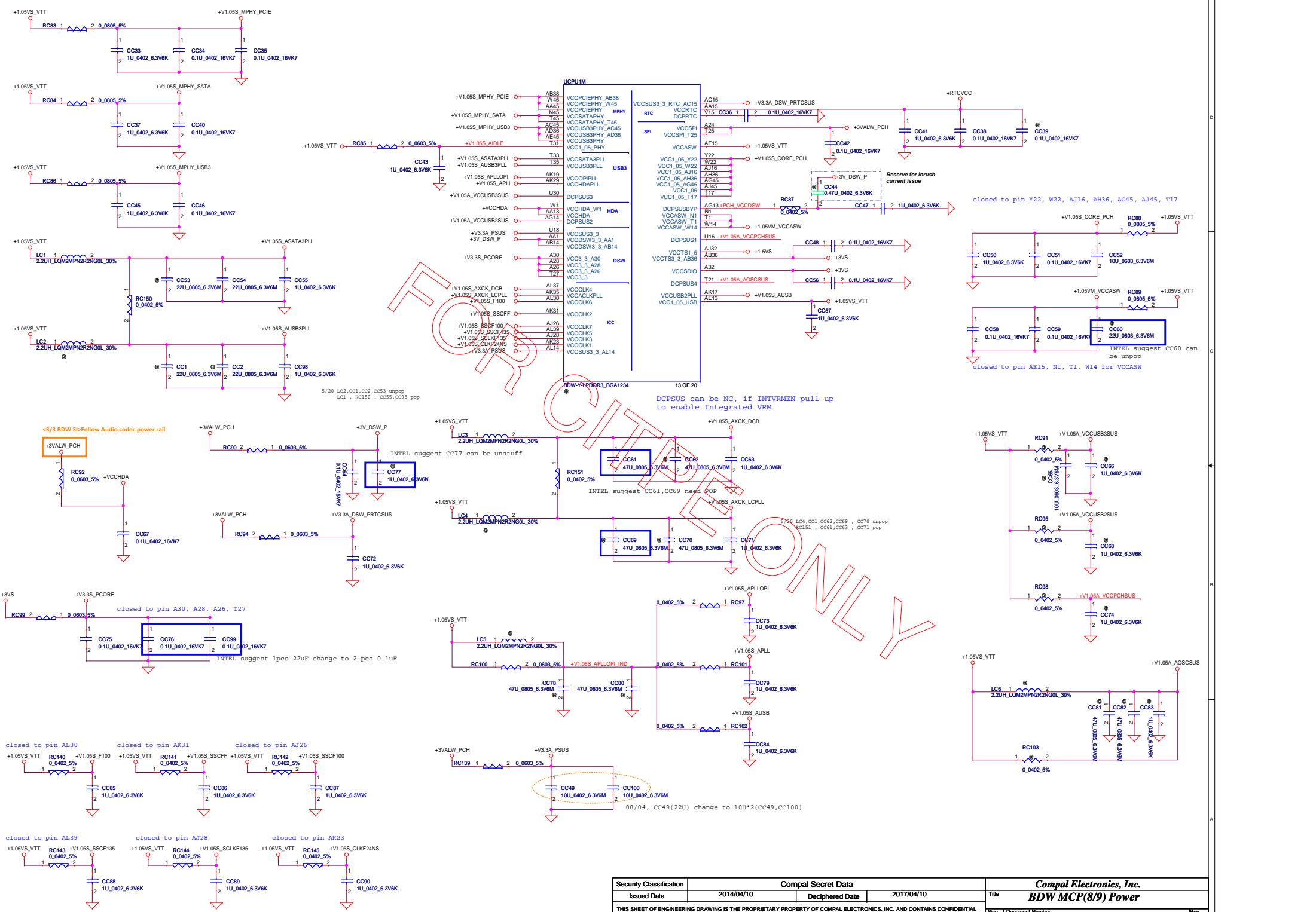
USB3RN176  
USB3RP176  
USB3TN176  
USB3TP176

USB3RN177  
USB3RP177  
USB3TN177  
USB3TP177

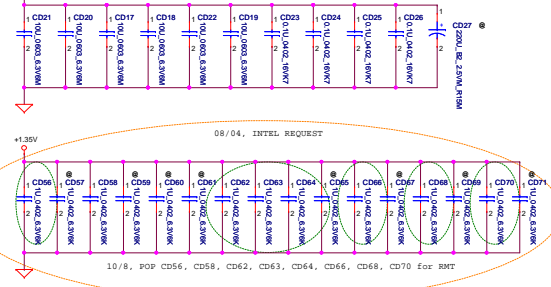
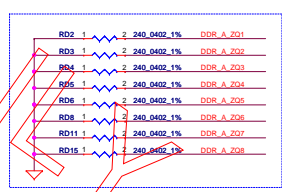
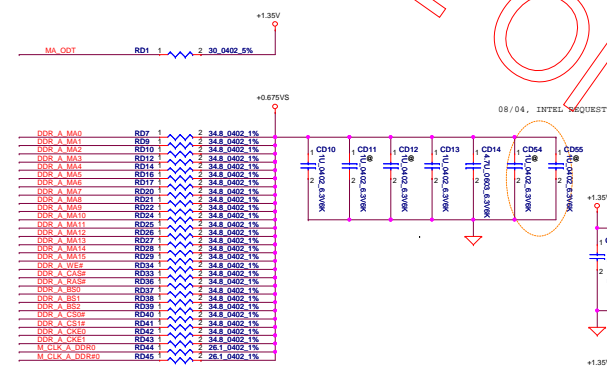
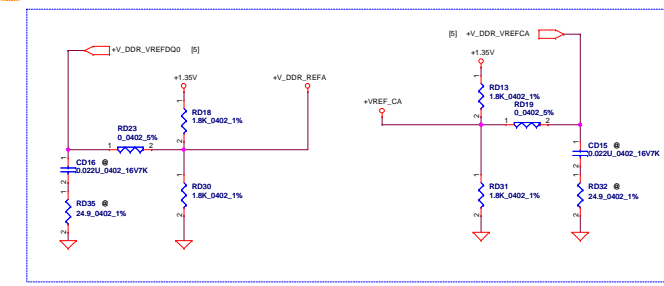
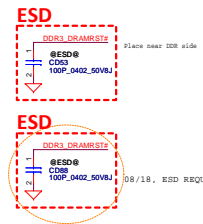
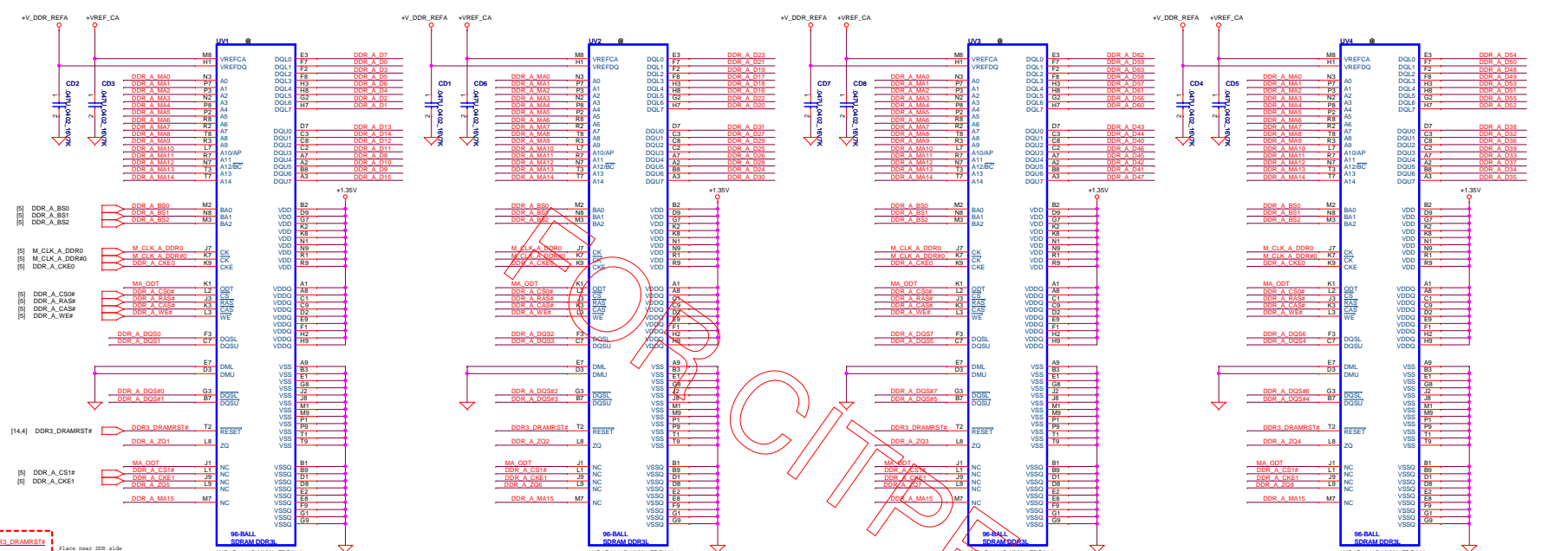
USB3RN178  
USB3RP178  
USB3TN178  
USB3TP178

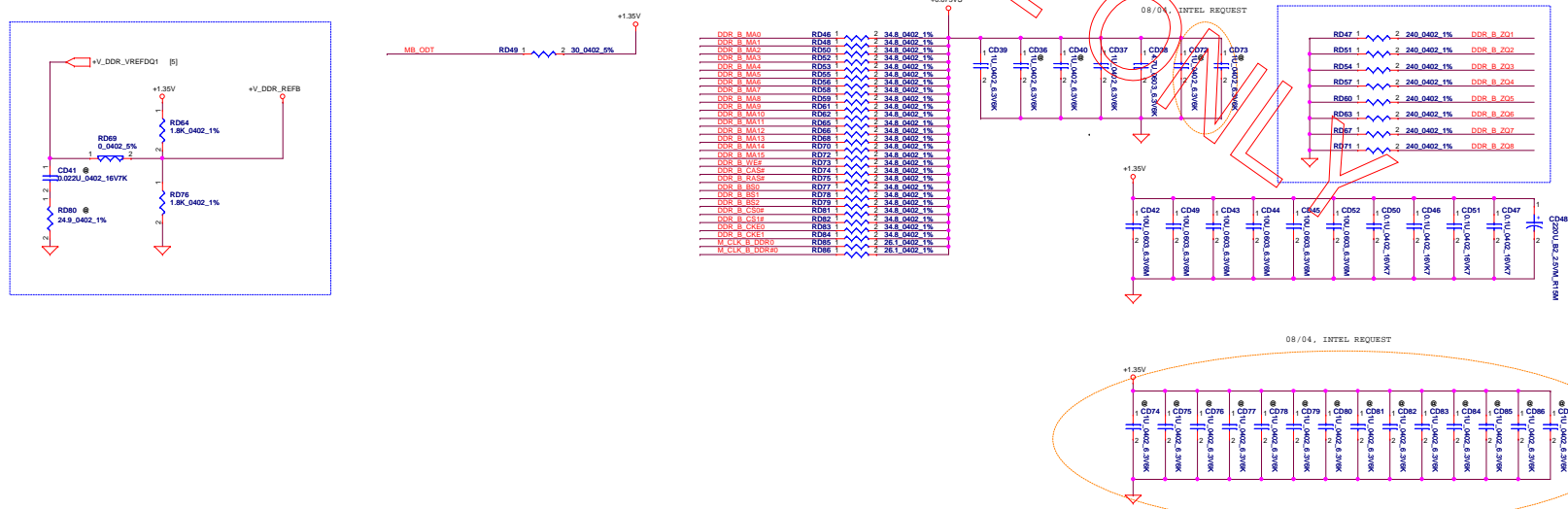
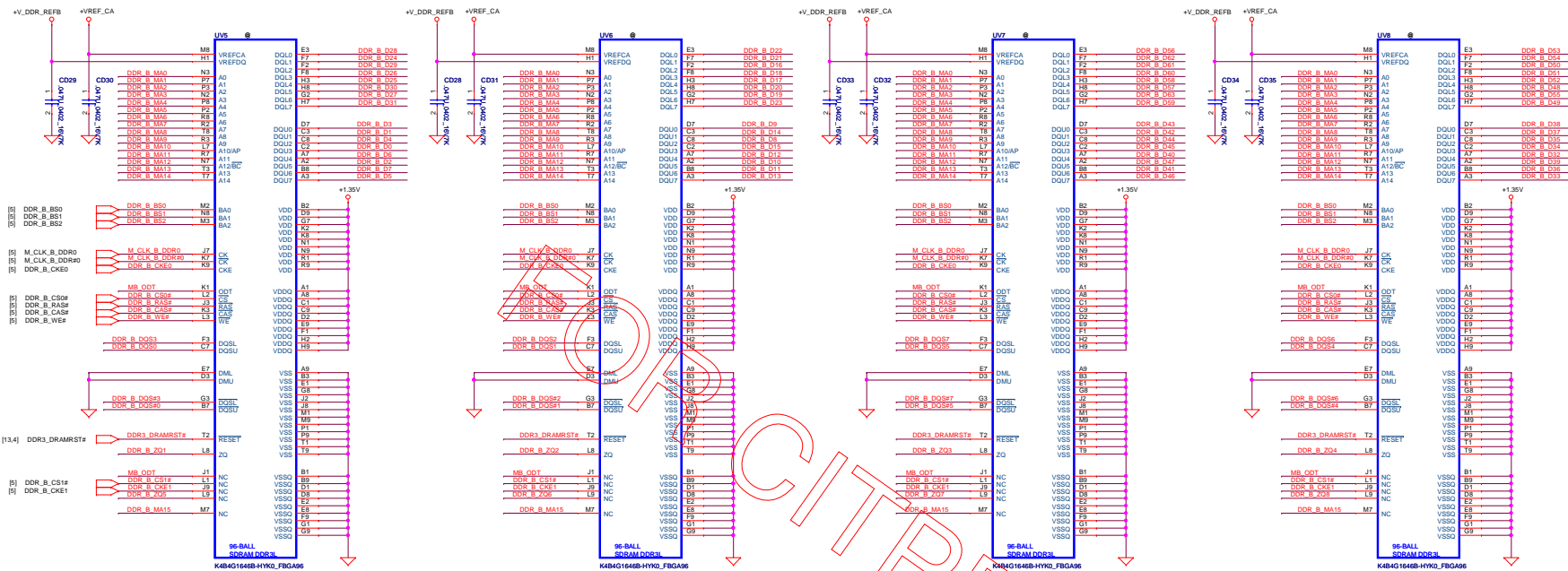
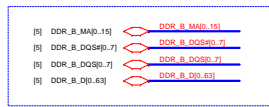
USB3RN179  
USB3RP



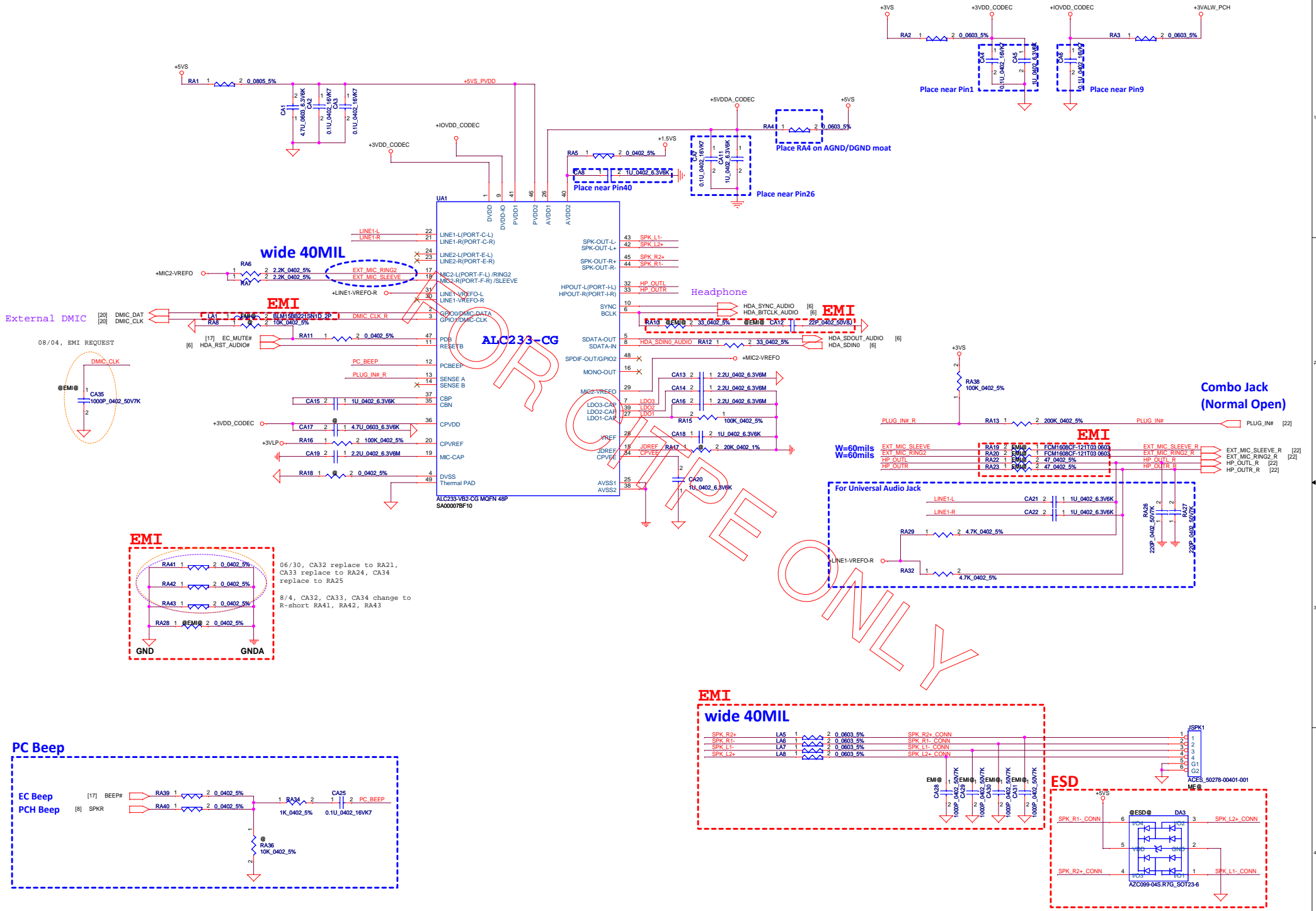






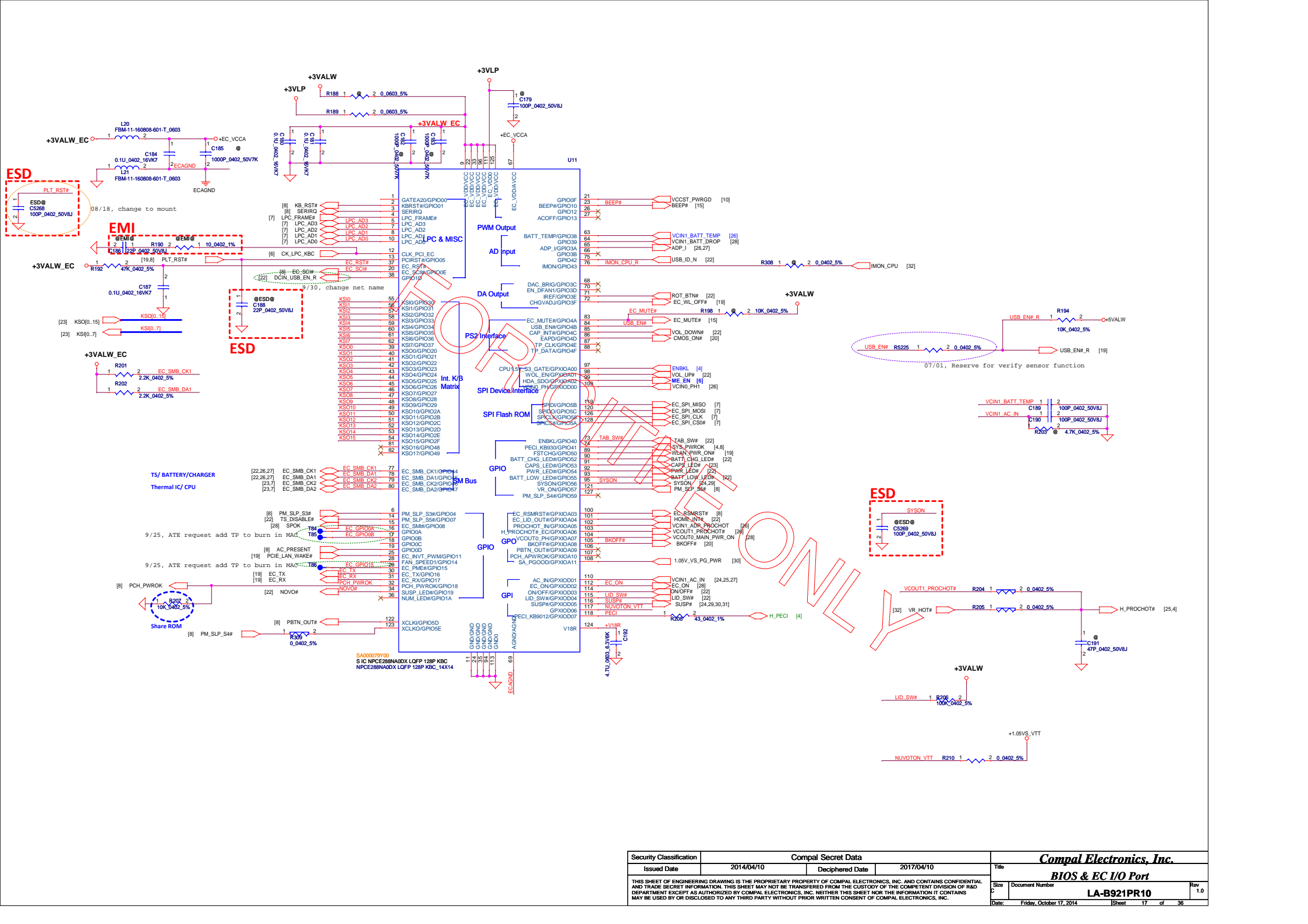




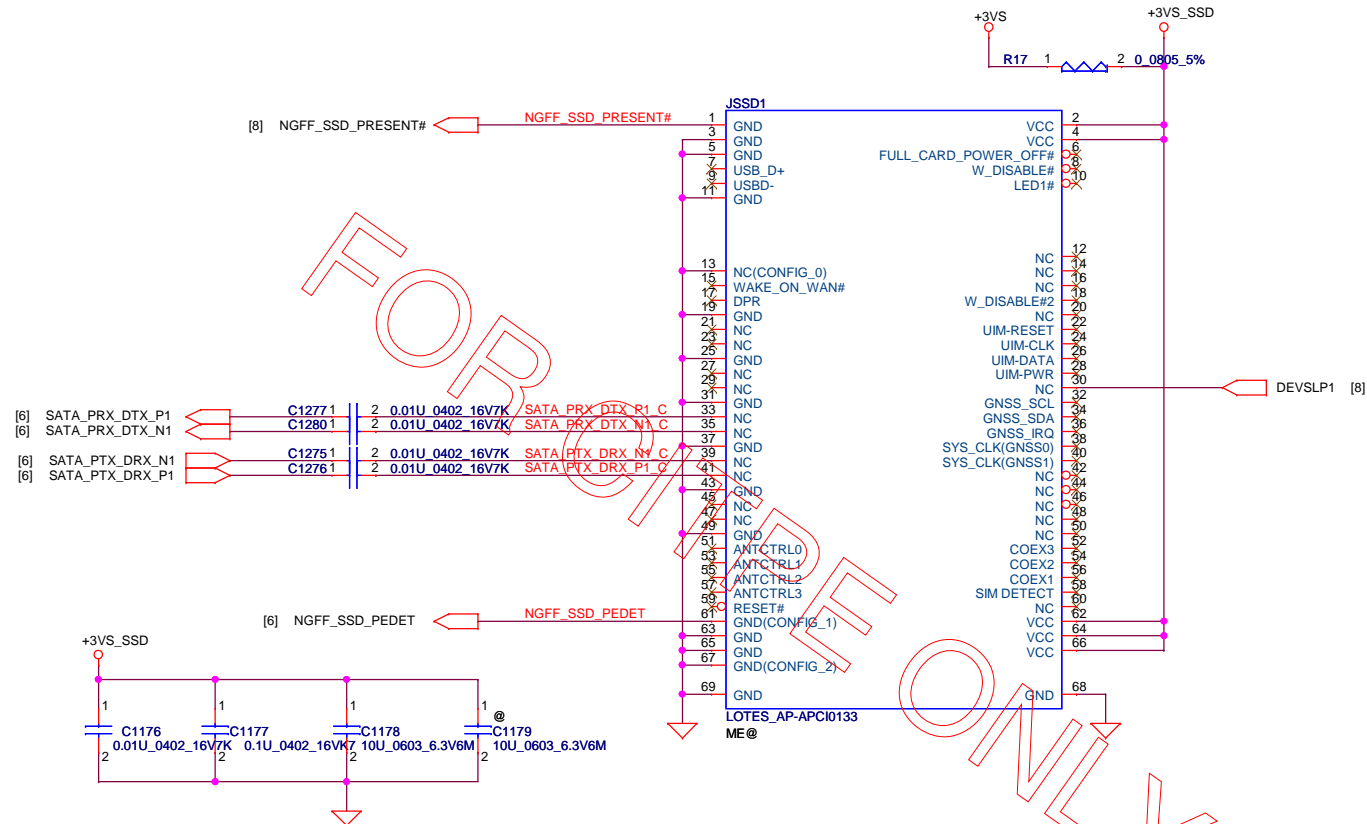






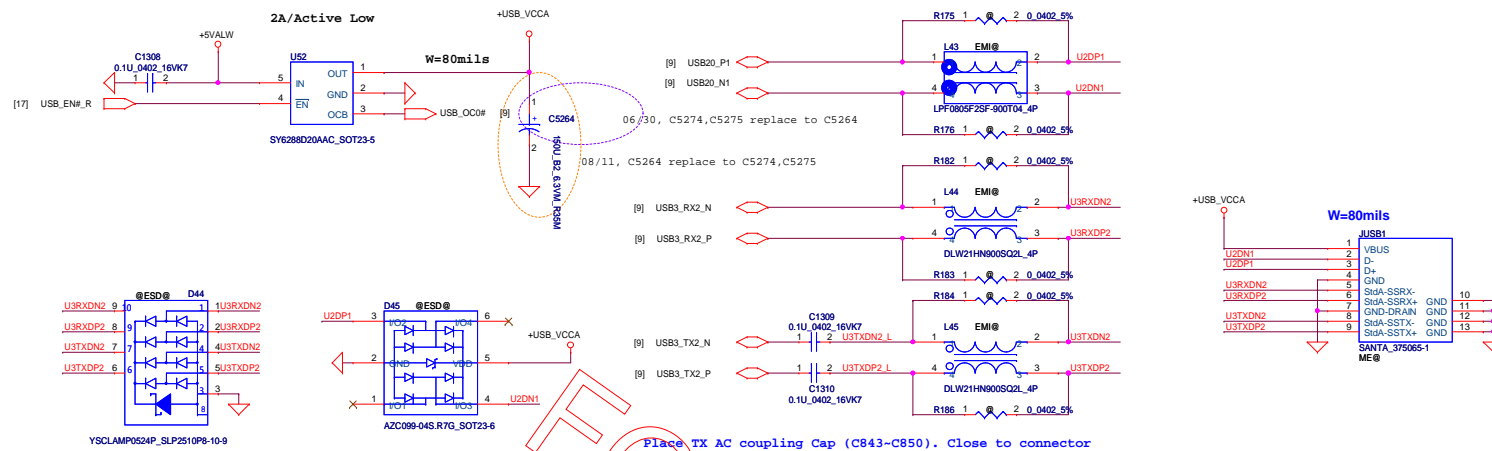


# NGFF for SSD(Key B)

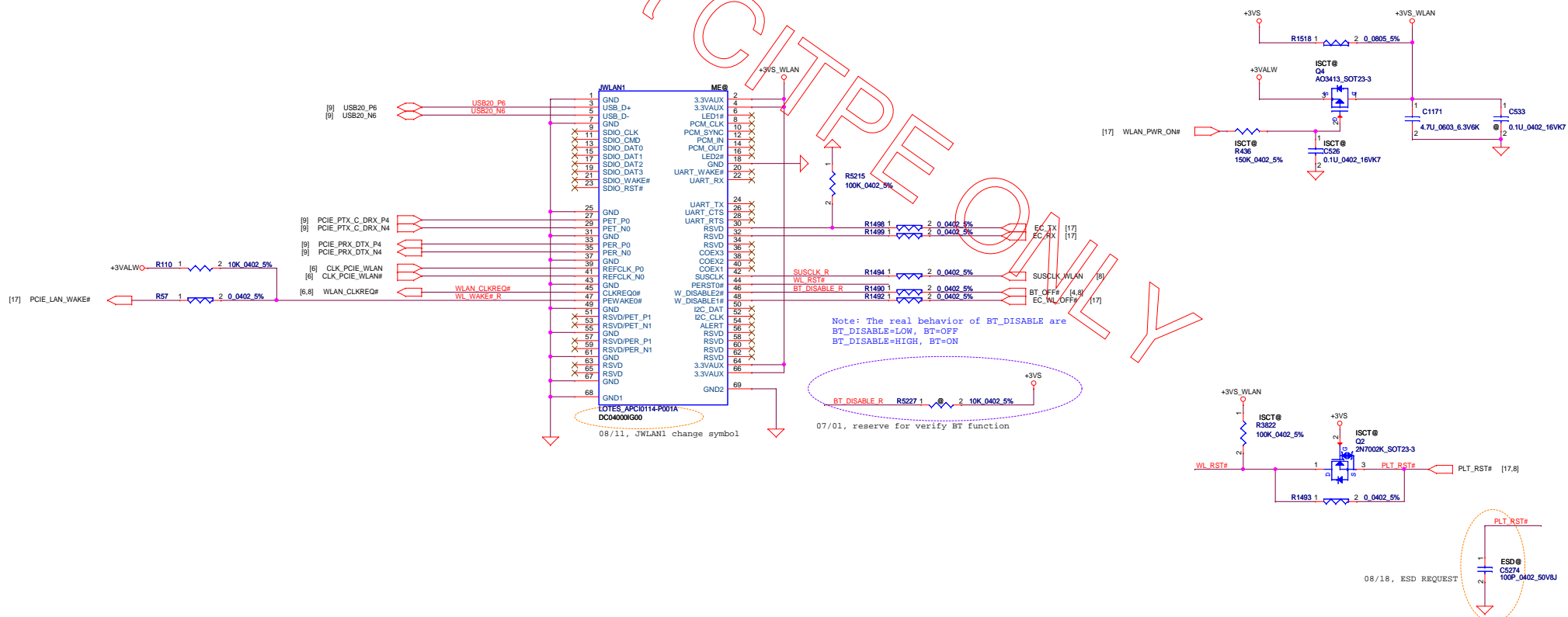


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	SSD
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B921PR10
				Date:	Friday, October 17, 2014
				Sheet	18 of 36

### USB 3.0 Conn.

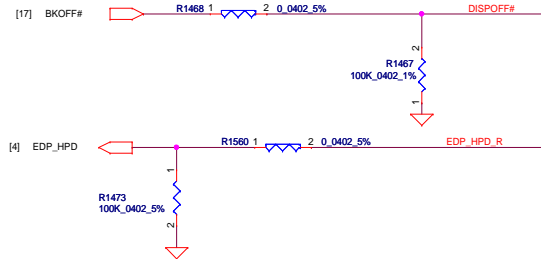
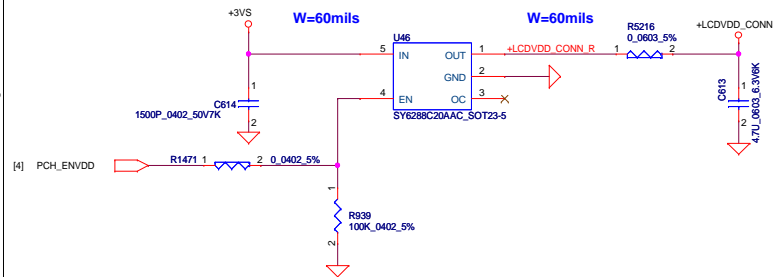


## NGFF for WLAN(Key E)

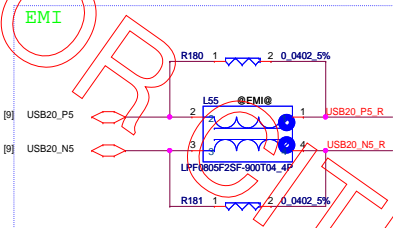
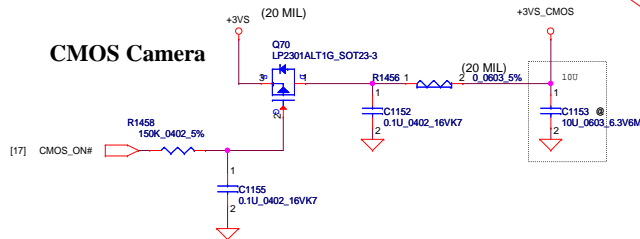


Security Classification		Compal Secret Data		<div> <div>Compal Electronics, Inc.</div> <div> <div>USB3.0/WLAN</div> <div> <div>LA-B921PRI0</div> <div>Rev 1.0</div> </div> </div> </div>	
Issued Date	2014/04/10	Deciphered Date	2017/04/10		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<div> <div>Title</div> <div>Size</div> <div>Document Number</div> <div>Date</div> </div>	
				<div> <div>Friday, October 17, 2014</div> <div>Sheet 19 of 36</div> </div>	

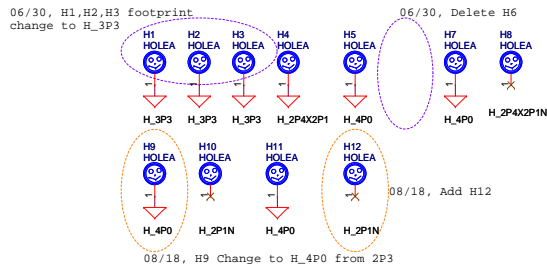
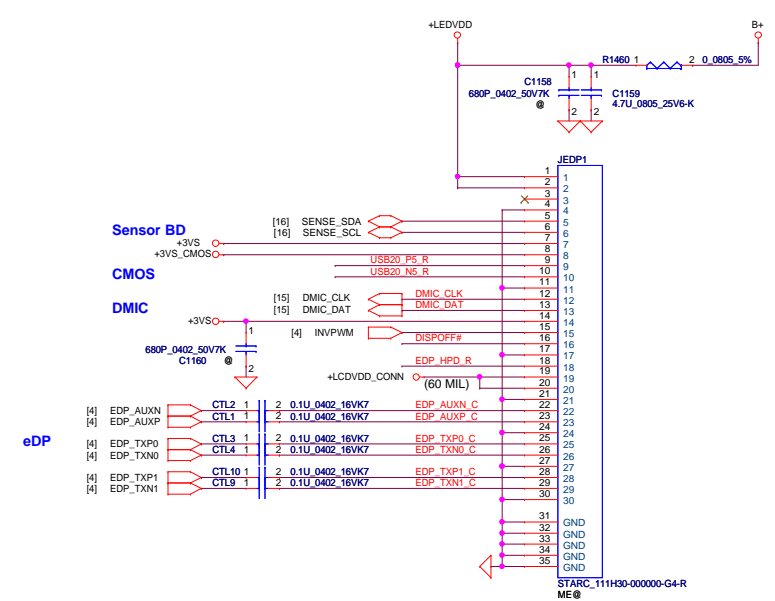
## LCD POWER CIRCUIT



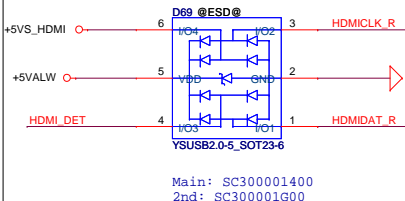
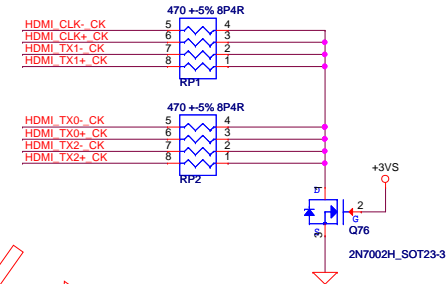
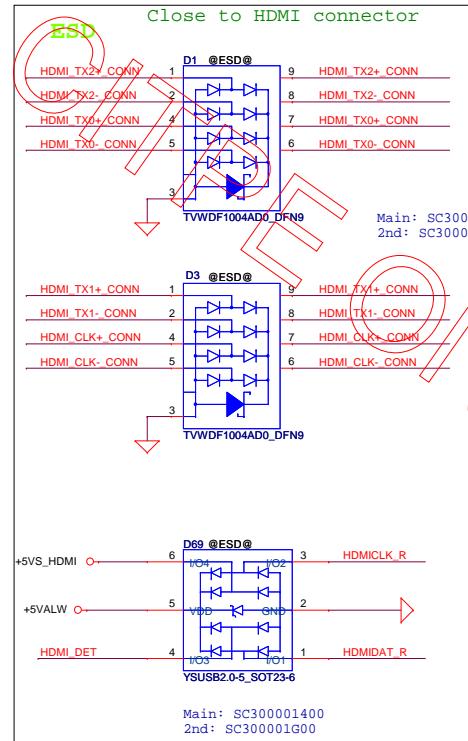
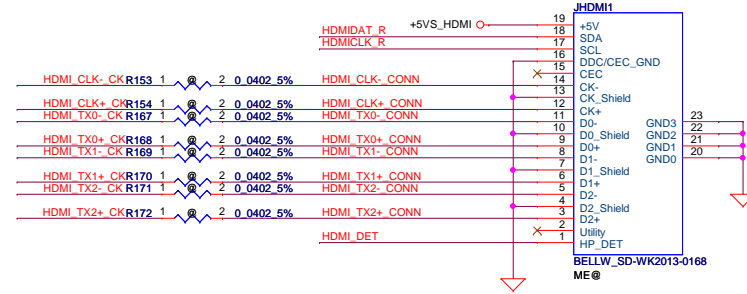
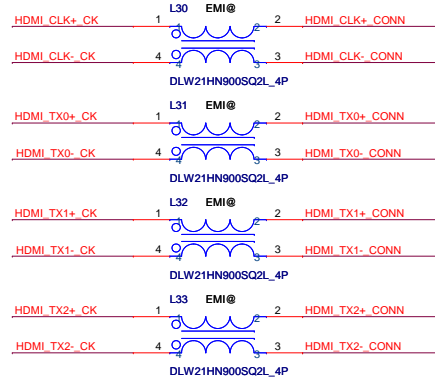
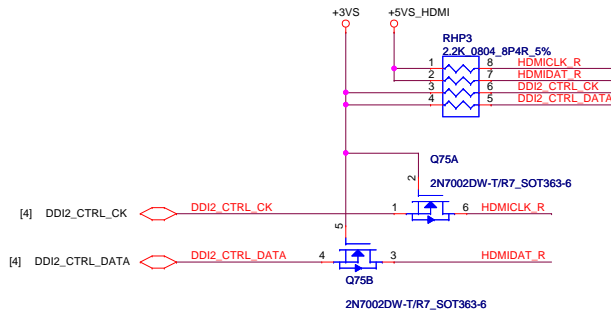
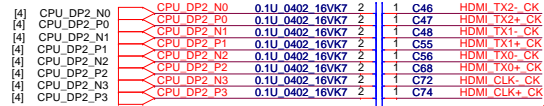
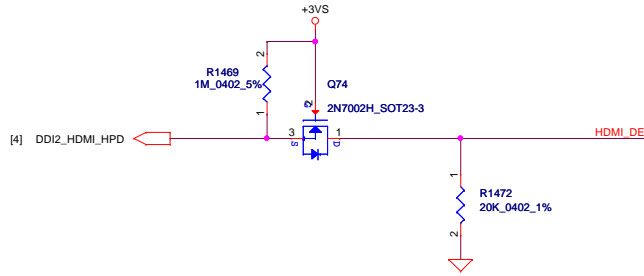
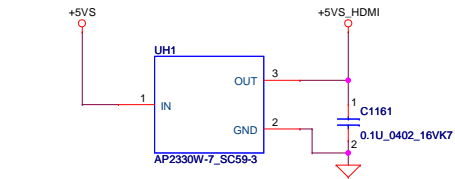
## CMOS Camera



## eDP PANEL/DMIC/COMS/SENSOR. Conn.

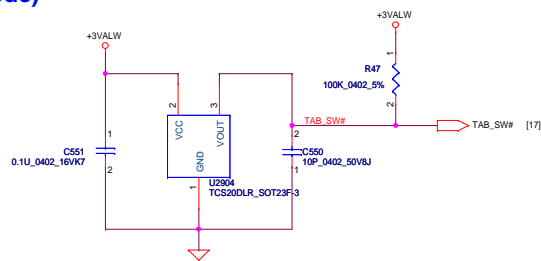


Security Classification		Compal Secret Data	
Issued Date	2014/04/10	Deciphered Date	2017/04/10
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			
Title		Compal Electronics, Inc.	
Size		eDP /DMIC/COMS/HOLE	
Customer		LA-B921PR10	
Date		Friday, October 17, 2014	
Sheet		20 of 36	

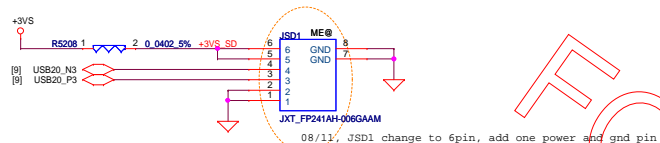


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	HDMI CONN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B921PR10
				Date: Friday, October 17, 2014	Rev 1.0
				Sheet 21 of 36	

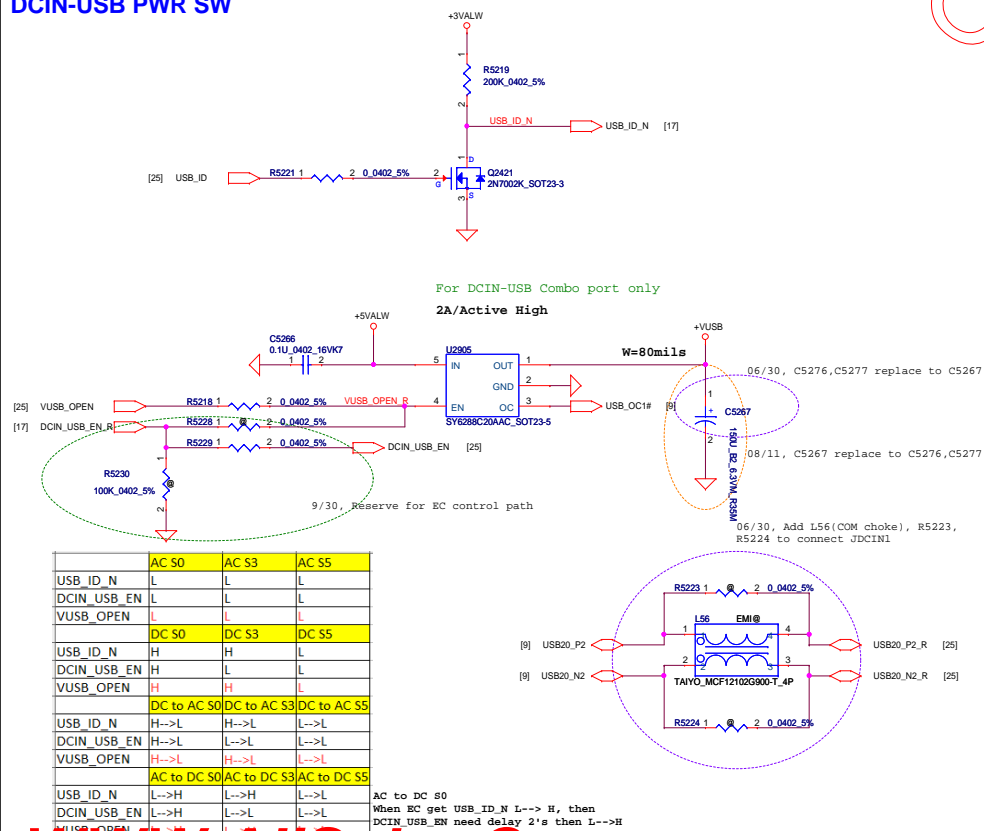
# Lid SW(Tablet Mode)



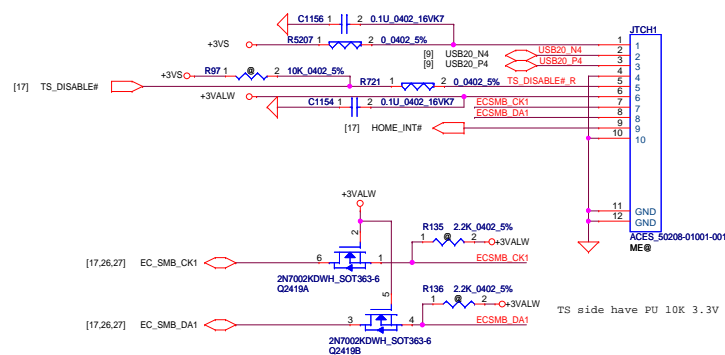
# SD Board



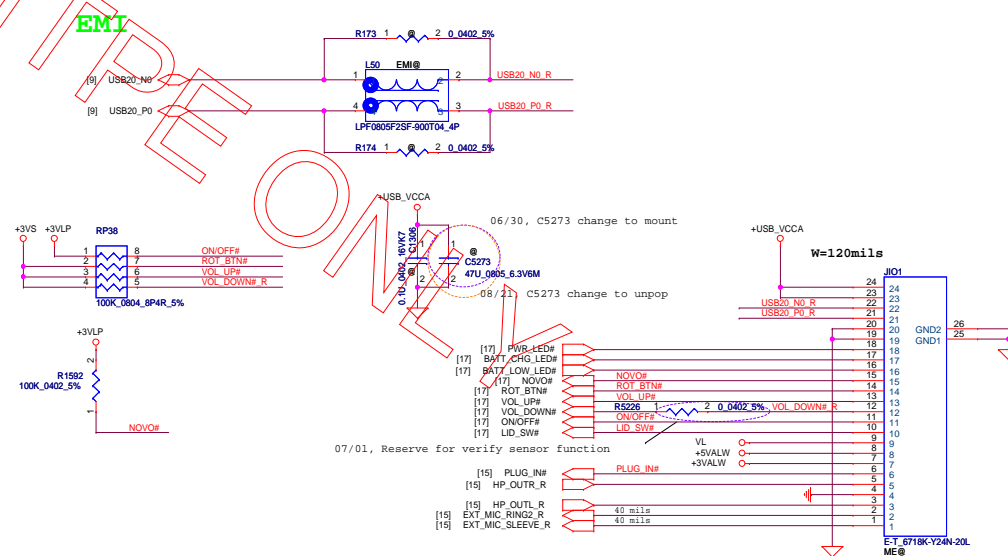
# DCIN-USB PWR SW



# Touch Panel



# I/O Board



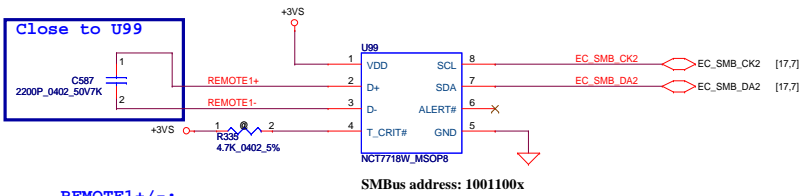
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>IO BD/ SD BD/TOUCH/LED/LID</b>		
				Size C	Document Number	Rev 1.0
				<b>LA-B921PR10</b>		
Date: Thursday, October 23, 2014				Sheet 22	of 36	



Thermal Sensor

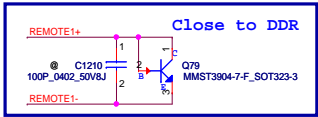
Keyboard

Close to U99

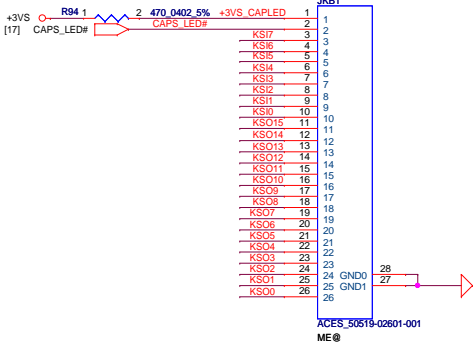
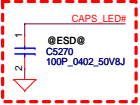


REMOTE1+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

Close to DDR

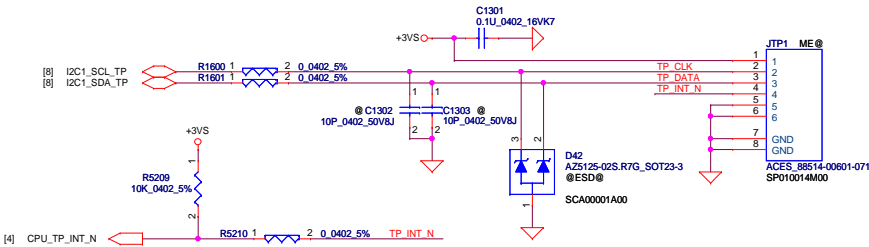


ESD



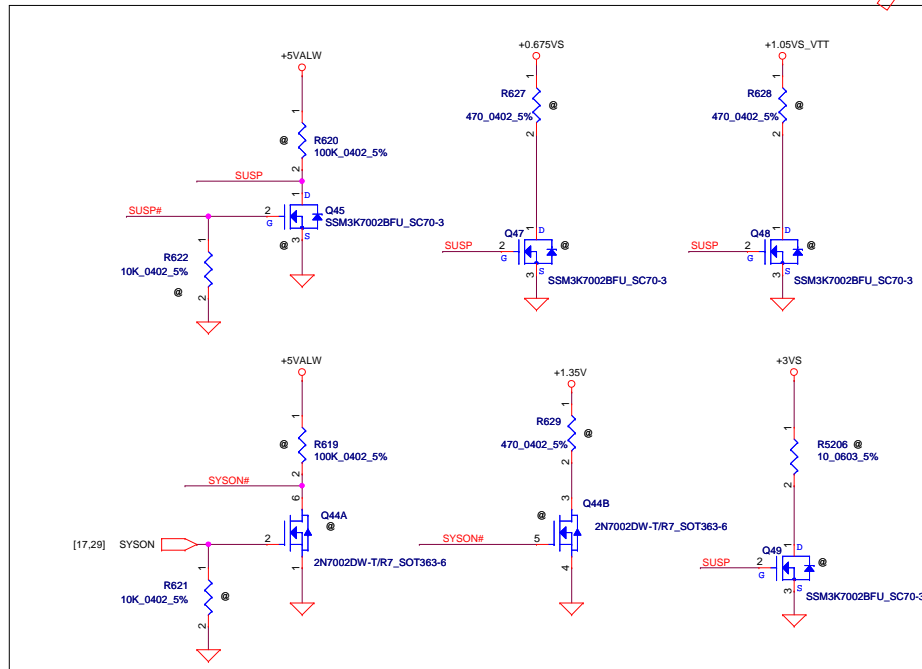
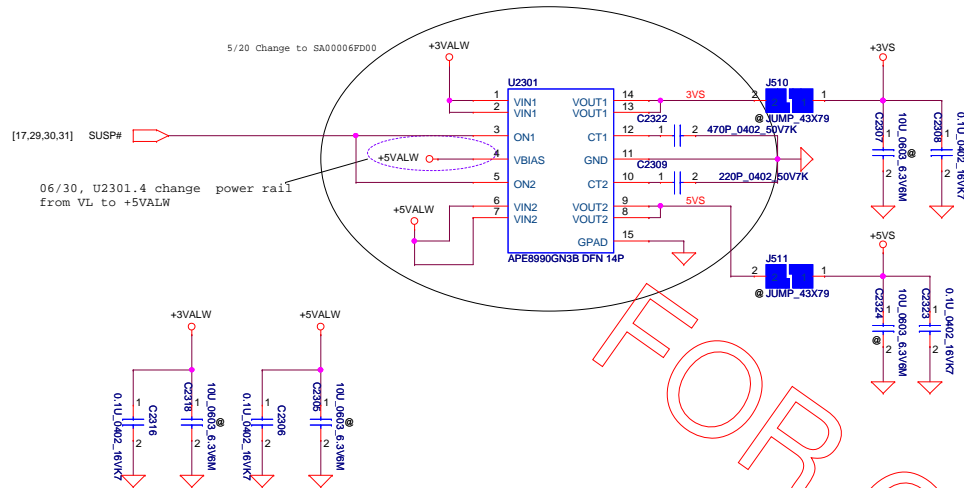
PIN1	+3VALW
PIN2	CAP_LED
PIN3	KS17
PIN4	KS16
PIN5	KS15
PIN6	KS14
PIN7	KS13
PIN8	KS12
PIN9	KS11
PIN10	KS10
PIN11	KS015
PIN12	KS014
PIN13	KS013
PIN14	KS012
PIN15	KS011
PIN16	KS010
PIN17	KS09
PIN18	KS08
PIN19	KS07
PIN20	KS06
PIN21	KS05
PIN22	KS04
PIN23	KS03
PIN24	KS02
PIN25	KS01
PIN26	KS00

Click Pad



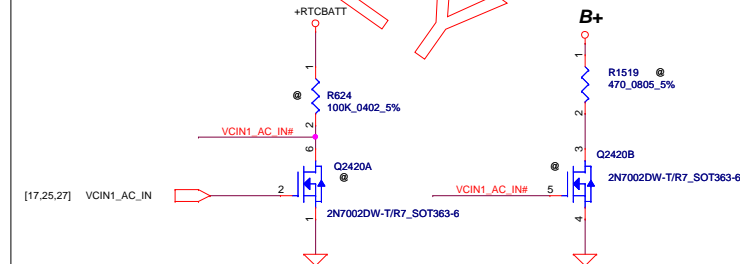
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	KB/TP/Thermal Sensor	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev
				LA-B921PR10		1.0
				Date: Friday, October 17, 2014	Sheet 23 of 36	

+5VALW TO +5VS  
+3VALW TO +3VS



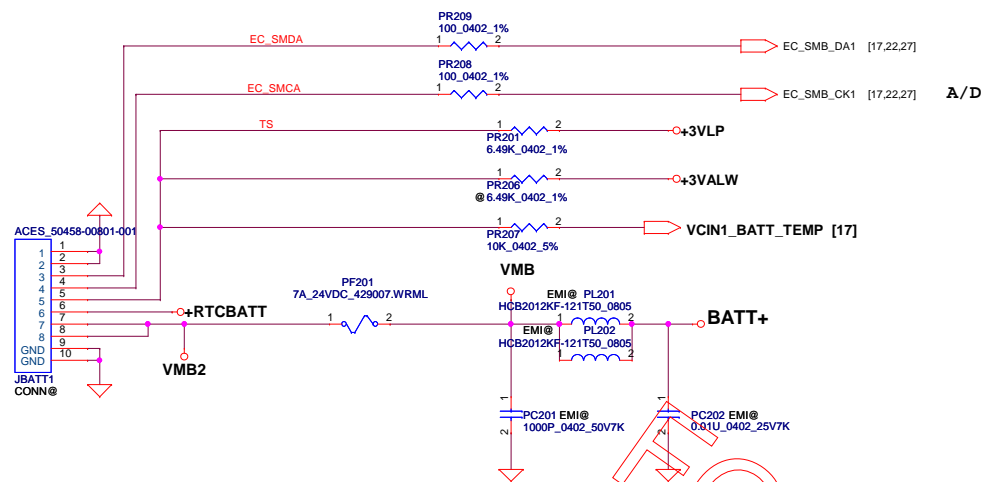
Use for panel sequence

**B+ discharger**



Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2014/04/10		Deciphered Date		2017/04/10		Title	
								DC V TO VS INTERFACE	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.									
Size		Document Number		LA-B921PR10		Rev		1.0	
Date:		Friday, October 17, 2014		Sheet		24		of 36	

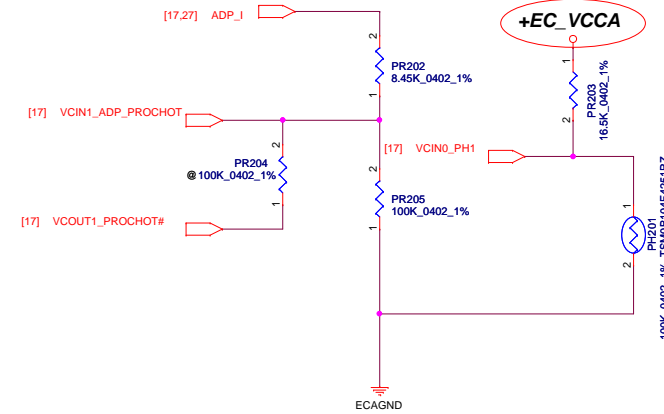




PH201 under CPU bottom side :  
CPU thermal protection at 93  $\pm$  3 degree C  
Recovery at 56  $\pm$  3 degree C

65W(UMA): 85W active W recovery

20120314  
Change to +EC\_VCCA from +3VLP

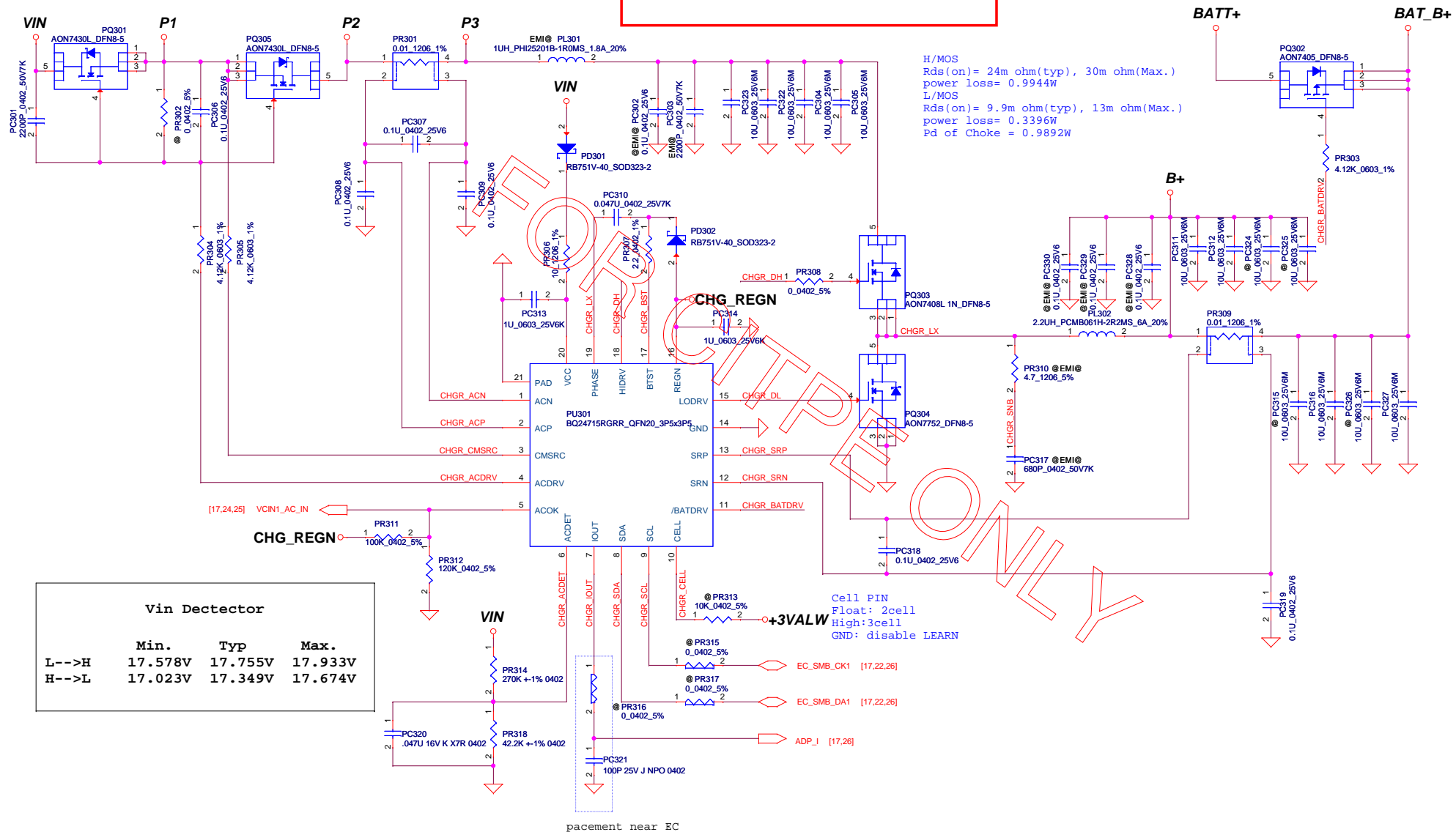


Security Classification		Compal Secret Data		Title	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				YOGA Paganini	1.0
				Date: Friday, October 17, 2014	Sheet 26 of 36

# Module model information

BQ24715\_V2.mdd

65W adapter support NVDC  
BQ24715 support 2, 3 cell  
BQ24717 for 4 cell

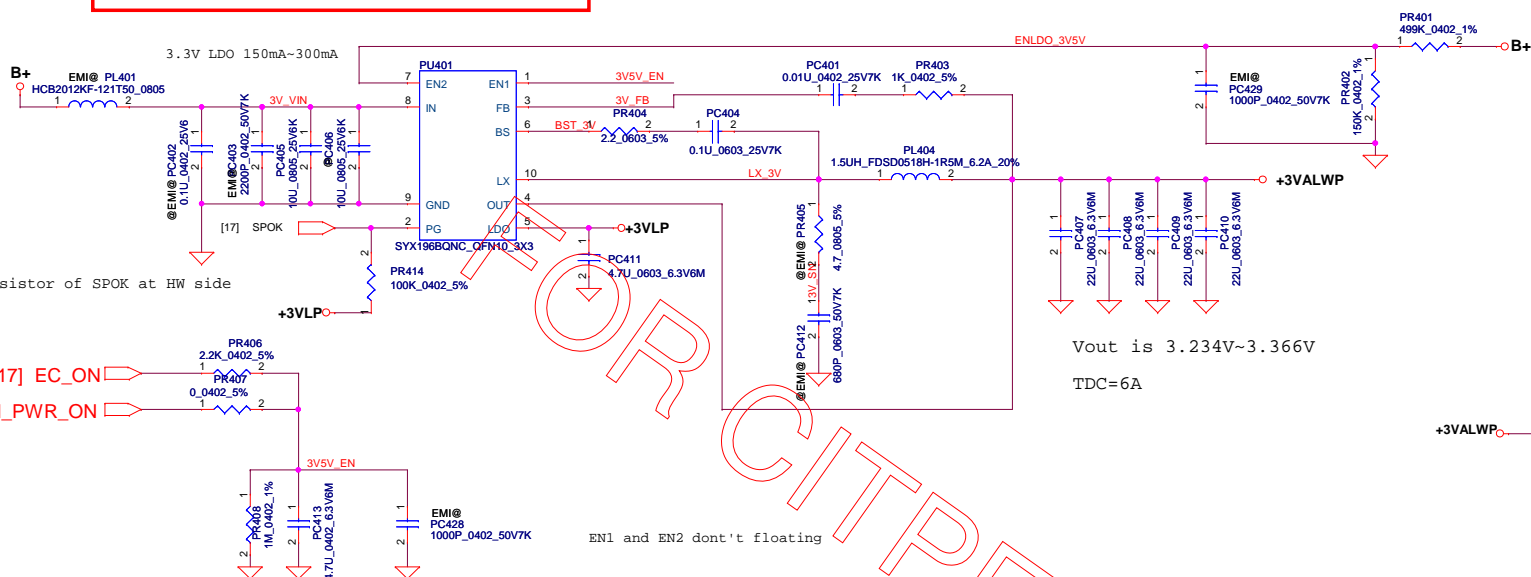


# Module model information

SYX196B\_V4.mdd

EN1 and EN2 don't floating

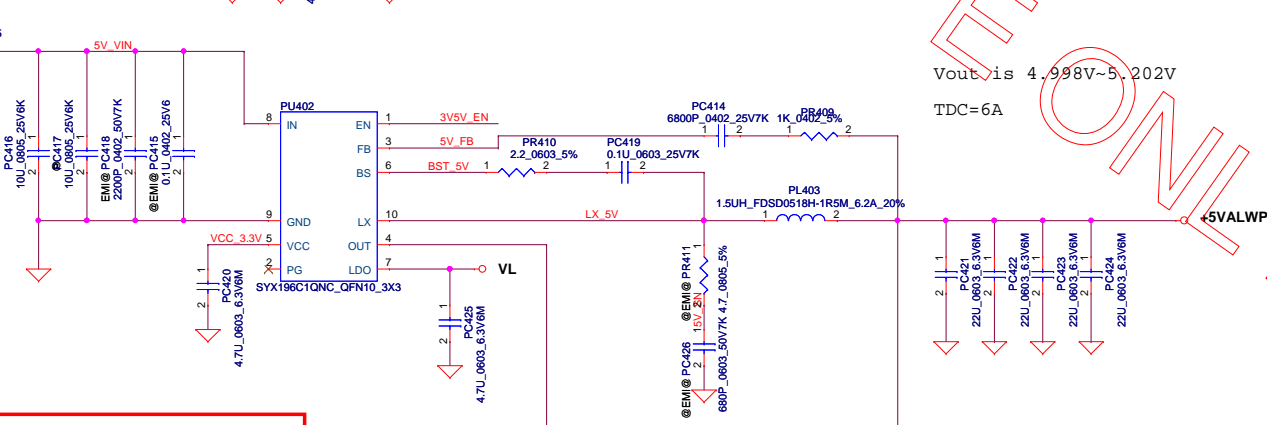
3.3V LDO 150mA~300mA



[17] EC\_ON

[17] VCOUT0\_MAIN\_PWR\_ON

B+ EMI@ PL402  
HCB2012KF-121T50\_0805



# Module model information

SYX196C\_V4.mdd

5V LDO 150mA~300mA

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				YOGA Paganini
				Rev 1.0
				Date: Friday, October 17, 2014
				Sheet 28 of 36

Compal Electronics, Inc.

PWR-3VALW/5VALW

YOGA Paganini

Date: Friday, October 17, 2014

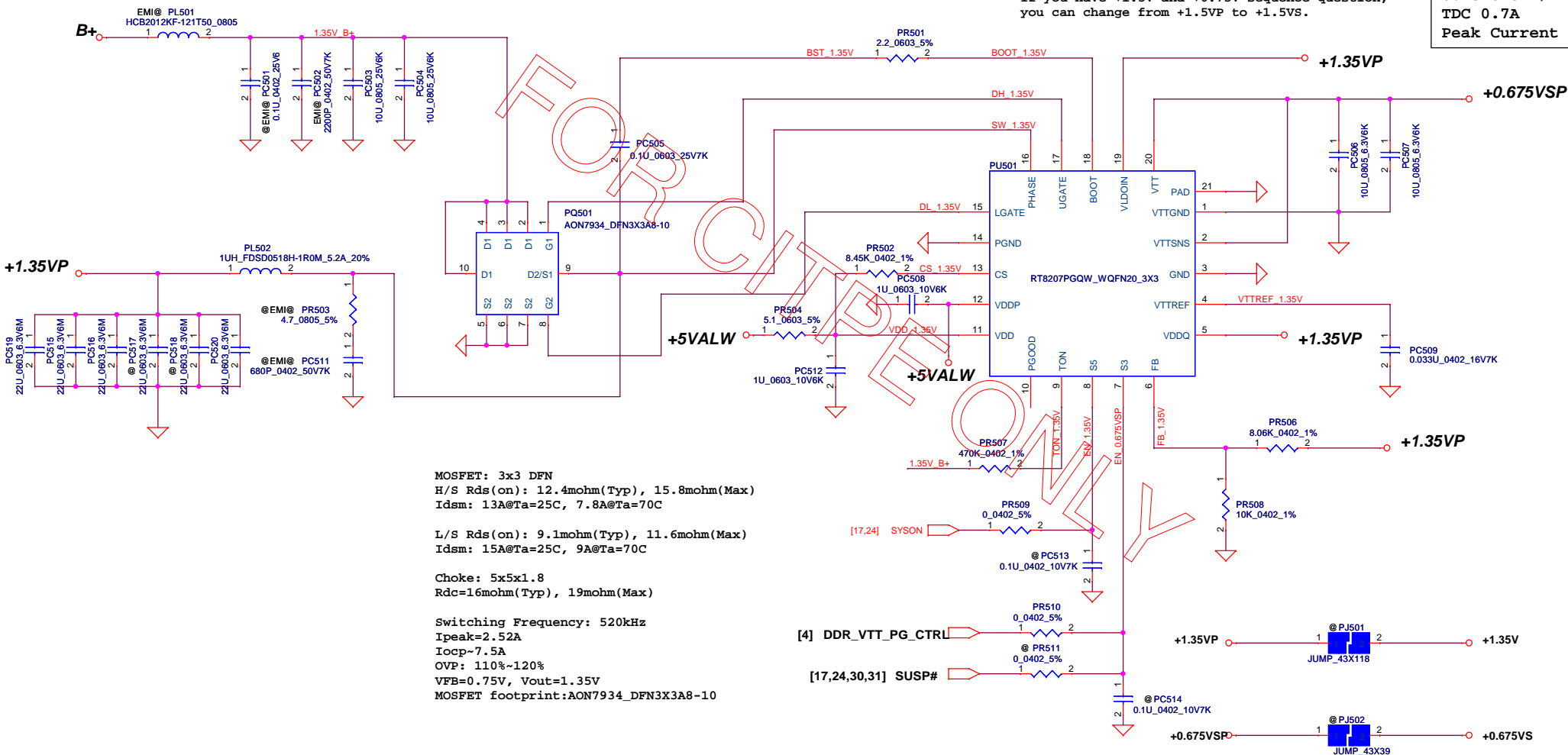
Sheet 28 of 36

# Module model information

RT8207M\_v1.mdd For Single layer  
RT8207M\_v2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.  
If you have +1.5V and +0.75V sequence question,  
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



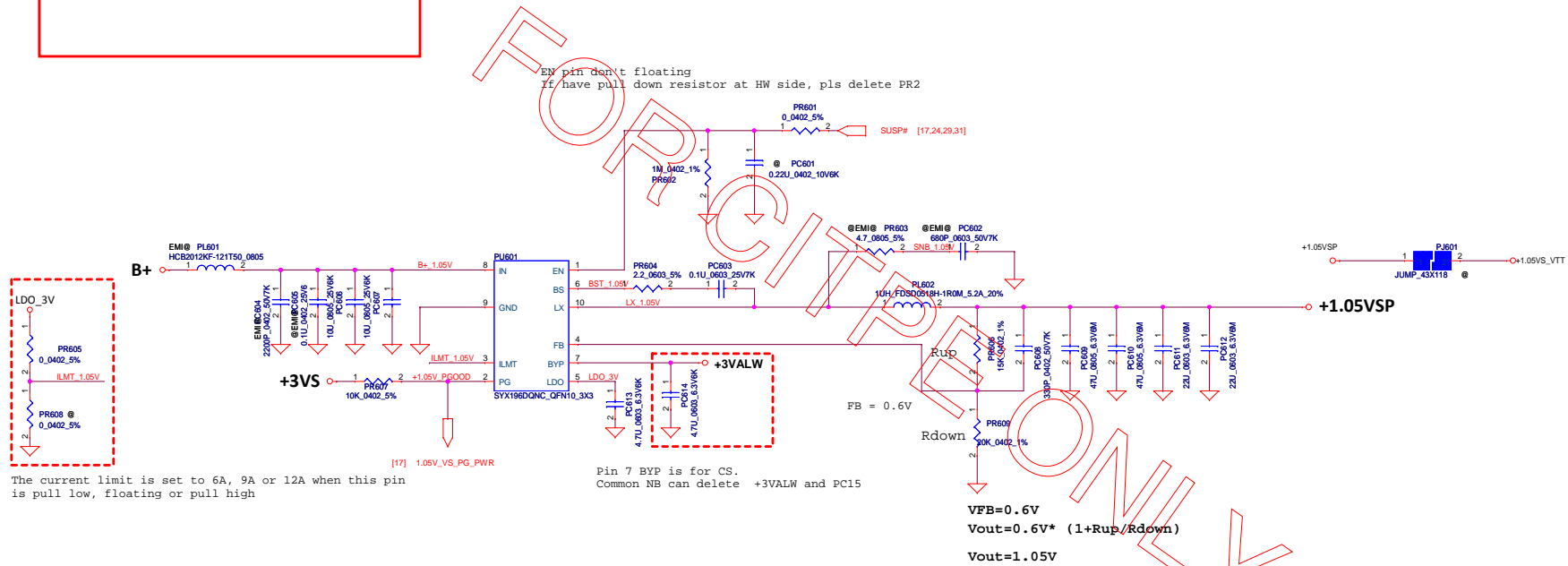
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	PWR-1.35V/0.675VS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	YOGA Paganini
				Date:	Friday, October 17, 2014
				Sheet	29 of 36
				Rev	1.0



# Module model information

SYX196D\_V3.mdd

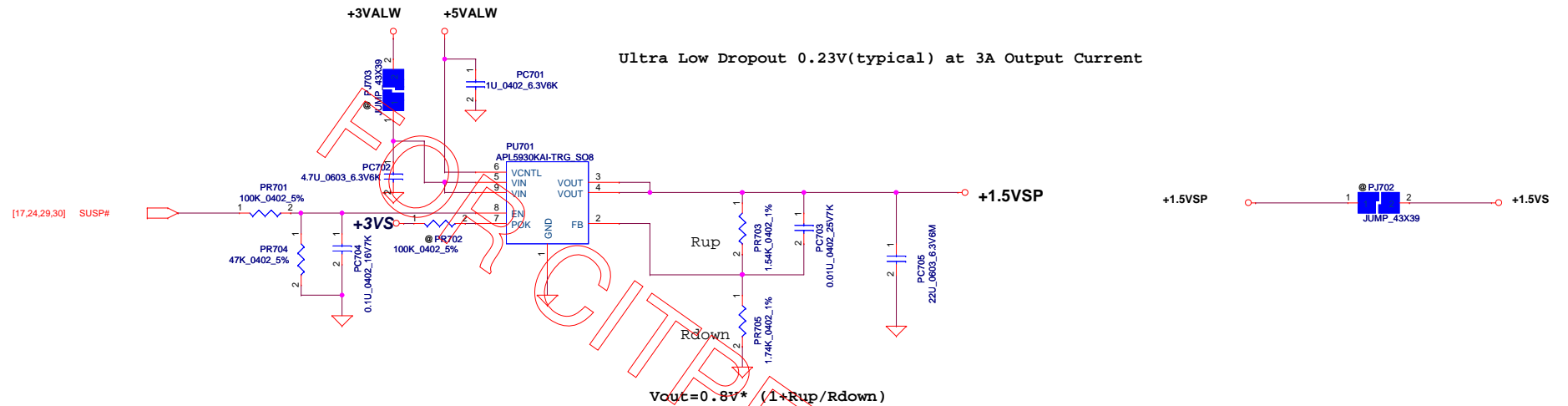
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-1.05VS
Size	Document Number	YOGA Paganini		Rev
C				1.0
Date:	Friday, October 17, 2014	Sheet	30	of 36

# Module model information

APL5930\_V2.mdd



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	PWR-1.5VS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	YOGA Paganini	1.0
				Date:	Friday, October 17, 2014	Sheet 31 of 36

Module model information:  
ISL95813\_V1A for IC module  
ISL95813\_V1B for SW module

Base on BDW PDDG Rev\_1.2

Location	4.5W	
	TDC 8A	
	MAX 18A	
	OCF 27A	
	Loadline=-2.0mV/A	Note
PR820	1.27K Ohm	OCF
PR816	909 Ohm	Droop
PC816	0.047uF	RC Match
PR803	73.2kOhm	PROG1
PR806	102kOhm	IMON
PC817	@	RC Filter

Dual MOS: AON6932A  
Rds(on):  
@Vgs=10V  
Q1=4.1mohm  
Q2=1.7mohm  
@Vgs=4.5V  
Q1=6.7mohm  
Q2=2.4mohm

Choke: 0.22uH (Size:7\*7\*1.8)  
Rdc=4.3m ohm +5%  
Heat Rating Current=14A

+1.05VS\_VTT Follow intel guideline

Note:  
VR\_SVID\_ALRT# Pull high on HW side

[10] VR\_SVID\_DAT

[10] VR\_SVID\_ALRT#

[10] VR\_SVID\_CLK

[10] VR\_ON

[10] VGATE

[17] IMON\_CPU

Note:  
VR\_HOT# Pull high on HW side

[17] VR\_HOT#

Over temperature protection:  
OTP Setting: 100C active  
Pin5 (NTC) voltage <0.88V, Protect  
Pin5 (NTC) voltage >0.92V, recovery

[10] VCCSENSE

[12] VSSSENSE

Local sense put on HW site

Note:  
PR803=73.2K  
=>Icc(max)=18A  
fsw=700KHz

Note:  
PR512=124K  
=>Slew rate=53mV/us  
Vboot = 1.7V

RC Match

OCF Setting

CPU\_B+

B+

+CPU\_CORE

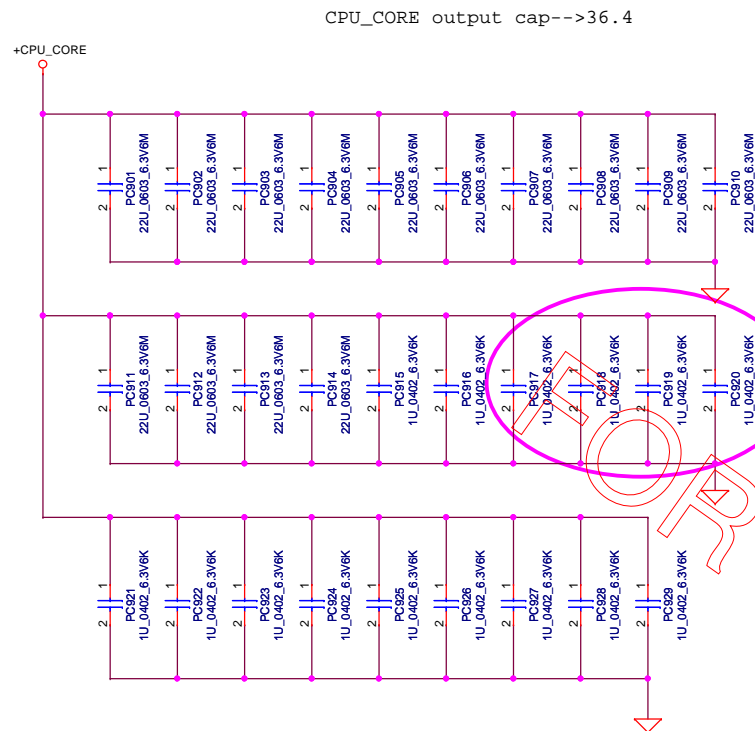


Compal Electronics, Inc.

PWR-CPU CORE

LA-B921PR10

Date: Friday, October 17, 2014 Sheet 32 of 36



30 X 22uF 0805  
2012/10/23  
check the output cap Qty!!!  
2012/10/24  
23 pcs 22uF and reserve 7 pcs  
2013/01/14  
22uF\*15; reserve 22uF\*5

2013/09/6 22U\_0603x17 + 22U\_0805x2

DRAFT

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	PROCESSOR DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				YOGA Paganini	
				Date:	Friday, October 17, 2014
				Sheet	33 of 36
				Rev	1.0

Item	Reason for change	PAGE	Modify List	Date	Phase
------	-------------------	------	-------------	------	-------

FOR CITPE ONLY

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-PIR	
				YOGA Paganini	
Date: Friday, October 17, 2014				Sheet 34 of 36	Rev 1.0

## Version change list (P.I.R. List)

Page 1 of 1  
for HW

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ME Request	P.20	H1,H2,H3 footprint change to H_3P3, Delete H6	2014-06-30	EVT-DVT	Pass
2	EMI request, for DCIN-USB port USB signal	P.22	Add L56(COM choke), R5223, R5224 to connect JDCIN1	2014-06-30	EVT-DVT	EA Pass
3	EMI request	P.15	CA32 replace to RA21, CA33 replace to RA24, CA34 replace to RA25	2014-06-30	EVT-DVT	Pass
4	EMI request	P.10	Reserve RC152 connect to JC1	2014-06-30	EVT-DVT	Pass
5	For fine tune I2C interface driving	P.8	RC130-RC133 change value to 2.2K ohm	2014-06-30	EVT-DVT	EA Pass
6	For ME Z-height limitation	P.19	C5274,C5275 replace to C5264	2014-06-30	EVT-DVT	EA Pass
7	For ME Z-height limitation	P.22	C5276,C5277 replace to C5267, C5273 change to mount	2014-06-30	EVT-DVT	EA Pass
8	For S5 power saving	P.24	U2301.4 change power rail from VL to +5VALW	2014-06-30	EVT-DVT	Pass
9	Reserve path for verify sensor function	P.22	Add 0 ohm R5226 to connect JIO1.12 and U11.85	2014-07-01	EVT-DVT	Pass
10	Reserve path for verify sensor function	P.17	Add 0 ohm R5225 to connect U52.4 and U11.84	2014-07-01	EVT-DVT	Pass
11	Reserve path for verify BT function	P.19	Add PU R5227 to connect BT_DISABLE_R and +3VS	2014-07-01	EVT-DVT	Pass
12	Follow Intel design guide	layout	Voiding the GND plane underneath the SATA signals pad of JSSD1	2014-07-01	EVT-DVT	EA Pass
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Z-high impact for thermal plate	P.11	CC49(22U)(0603) change to 10U*2(CC49,CC100)(0402)	2014-08-13	DVT-PVT	Pass
2	Z-high impact for thermal plate	P.10	CC26, CC27, CC28, CC30 change to 0402 type	2014-08-13	DVT-PVT	Pass
3	Reserve for Intel request	P.13	ADD CD54, CD55, CD72, CD73 connect to +0.675VS	2014-08-13	DVT-PVT	
4	Reserve for Intel request	P.13 P.14	ADD CD56-CD71,CD74-CD87 connect to +1.35V	2014-08-13	DVT-PVT	
5	Reserve For EMI request	P.15	ADD CA35 connect to DMIC_CLK	2014-08-13	DVT-PVT	
6	solve plug in/out USB device auto shutdown issue	P.19 P.22	C5264 replace to C5274,C5275; C5267 replace to C5276,C5277	2014-08-13	DVT-PVT	Pass
7	For EMI/Audio request, solve audio noise issue	P.15	CA32, CA33, CA34 change to RA41, RA42, RA43	2014-08-13	DVT-PVT	Pass
8	ME request, for FFC 夾持力 issue	P.22	JSD1 connector change symbol 4pin to 6pin	2014-08-13	DVT-PVT	Pass
9	For DFB request	P.19	JWLAN1 change symbol	2014-08-13	DVT-PVT	Pass
10	Reserve For ESD request		Add C5274, CC101, CC102, CD88, PC328, PC329, PC330, PC428,PC429	2014-08-18	DVT-PVT	
11	For ME request	P.20	Fix hole H9 Change to H_4P0, Add H12	2014-08-18	DVT-PVT	
12	For ME request	layout	JEDP1 change location placement	2014-08-18	DVT-PVT	Pass
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ATE request reserve Test point to burn in MAC	P.17	Add T84,T85,T86	2014-09-25	PVT-SOVP	
2	For ME request	layout	JEDP1 change location placement(move down 2mm)	2014-09-25	PVT-SOVP	Verify on SOVP
3	Reserve DCIN USB power SW EC control path	P.22	Add R5228,R5229,R5230 to connect U2905, U11, PD103	2014-09-30	PVT-SOVP	
4	Reserve for ESD protect	P.25	Add DCIN_USB_EN connect to PD105	2014-09-30	PVT-SOVP	

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	
				HW PIR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	Rev 1.0
				Date	Friday, October 17, 2014
				Sheet	35 of 36

# Paganini Power Sequence

